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Precise constant current source for BZV10, 1N821 and BZX90 series voltage reference diodes

R. S. Babbs
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UDC 621.316.721[621.382.232]

A simple constant current source intended primarily for use with BZV10, BZX90, and 1N821 series voltage reference diodes is described. Operating from a single positive supply, the circuit utilises an operational amplifier, four resistors, and the reference voltage of the diode itself to control the reference current. For BZV10 series diodes, the circuit maintains the reference current constant to within 1μA (0·05%) for supply voltages between 10 and 20V, temperatures between 0 and 70°C, and output currents between 0 and 10mA. For BZX90 series diodes, the control of the reference current is better than 11μA (0·15%) for the same supply voltage and output current ranges, and for temperatures in the range 25 to 100°C.

INTRODUCTION

The BZV10, 1N821, and BZX90 series of voltage reference diodes have been designed to meet the need for rugged reference sources with low temperature coefficients. They can be used in place of standard cells in measuring equipment such as digital voltmeters and in regulated power supplies. The reference voltage given by the BZV10 and BZX90 series is 6·5V±5%, and that given by the 1N821 series is 6·2V±5%. The BZV10 series operates at a nominal reference current of 2mA, and the 1N821 and BZX90 series operate at 7·5mA. Because the diodes have finite differential resistances and their temperature coefficients may vary with current, it is necessary to maintain the reference current at a fixed value close to the nominal, and independent of changes in supply voltage, temperature and load. This article describes a differential amplifier constant current source suitable for use with BZV10, 1N821, and BZX90 series diodes.

BZV10, 1N821, AND BZX90 SERIES

All three series are manufactured using a multiple chip technique and are identical in construction. Each device consists of a DO–35 encapsulation containing two diodes on separate chips, connected back-to-back as shown in Fig. 1. One chip with a reference voltage of about 5·5V and a positive temperature coefficient operates in the reverse direction, and the other, with a negative temperature coefficient, operates in the forward direction. In this way, the temperature coefficients of the chips compensate each other to give a device with a very low overall temperature coefficient.

Voltage changes with temperature

Reference diodes are generally characterised using the 'box method'. That is, for a given type, the maximum change in reference voltage ΔV_{REF} over a specified temperature range and at a specified test current I_{REF} is guaranteed to lie within two defined boundaries. (The voltage change is referred to the voltage at a fixed temperature). For the BZV10 and 1N821 series, the magnitude of ΔV_{REF} is the only criterion used for classification. No account is taken of possible changes in temperature coefficient between the two boundaries. For the BZX90 series, however, limits are also specified for the maximum temperature coefficient at all temperatures in the operating range, in addition to the normal ΔV_{REF} limits set by the boundaries of the box. Therefore, for applications requiring control of both voltage change and rate of voltage change with temperature, use of the BZX90 series is recommended.

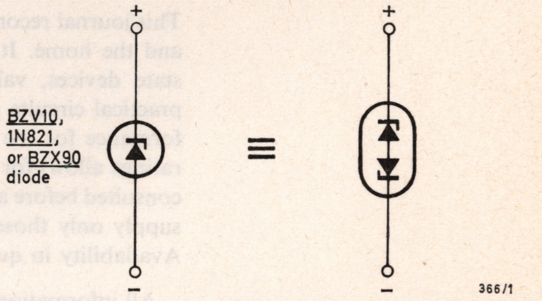

Fig. 1—Back-to-back construction of BZV10, 1N821, and BZX90 series

Table 1 gives the maximum voltage excursions for the BZV10 series over the temperature range 0 to +70°C, and for the 1N821 and BZX90 series over the temperature range −55 to +100°C. It also gives the temperature coefficient limits for the BZX90 series. The values quoted are for constant operating currents of 2mA for the BZV10 series and 7·5mA for the 1N821 and BZX90 series.

Changes of voltage with current

The most important factor governing the stability of the reference voltage of a reference diode is the diode current I_{REF}. If I_{REF} changes, V_{REF} changes because of the direct effect of the current change in the finite differential resistance of the diode r_Z. Furthermore, the temperature coefficient of voltage S_Z is a function of I_{REF}. Thus, any change in I_{REF} will result in a different value (higher or lower) of ΔV_{REF} for a given change in temperature ΔT. Although the absolute value of I_{REF} should remain in the limits set by the published data, the stability of I_{REF} is of far greater importance, particularly for those diodes with narrow maximum voltage change limits; that is, those with the higher type numbers in each series. For example, the maximum value of r_Z for the BZV10 series is 50Ω. Therefore a change of 10μA in I_{REF} can result in a change in V_{REF} of 0·5mV. For the BZV10, for which ΔV_{REF} max is 46mV, this change is only 1% of the total. For the BZV14, however, for which ΔV_{REF} max is 2·3mV, 0·5mV is about 20% of the total.

TABLE 1

Maximum voltage changes for BZV10, 1N821, and BZX90 series

Type	Max voltage change (0 to 70°C) (mV)	Max voltage change (−55 to +100°C) (mV)	Temperature Coefficient (%/deg C)
BZV10	±46		Not applicable
BZV11	±23		
BZV12	±9·0		
BZV13	±4·6		
BZV14	±2·3		
1N821		±96	Not applicable
1N823		±48	
1N825		±19	
1N827		±9	
1N829		±5	
BZX90		±96	0·01
BZX91		±48	0·005
BZX92		±19	0·002
BZX93		±9	0·001
BZX94		±5	0·0005

It is thus clear that there is a need to closely control the current and ensure that it is independent of variations in supply voltage, load, and temperature, and is stable with time. The constant current circuit described in this article is designed to meet this need.

CONSTANT CURRENT SOURCE

Basic Circuit

The starting point is a grounded-load, voltage-controlled current source in which the load current is a direct function of the control voltage, V_{in}. It uses an operational amplifier and the circuit diagram is shown in Fig. 2. Resistor R_I is the current limiting resistor. If both R_4 and R_2 are much greater than R_L, and $R_4/R_3 = R_2/R_1$, and if the amplifier has very high voltage gain, then the load current I_L is given by:

$$I_L = \frac{1}{R_I}\cdot\frac{R_2}{R_1}\cdot V_{in}, \qquad \ldots(1)$$

and is independent of R_L and the amplifier supply voltages.

Load resistor replaced by reference diode

If in Fig. 2 the load resistor is replaced by a voltage reference diode, the circuit becomes that shown in Fig. 3. The current I_{REF} through the diode is then a direct function of V_{in} and will remain constant if V_{in} remains constant.

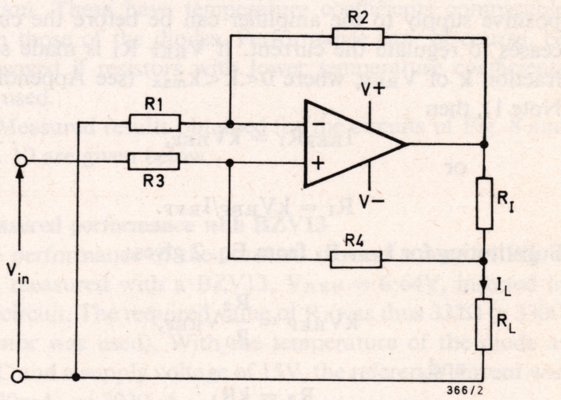

Fig. 2—Basic circuit of voltage-controlled current source

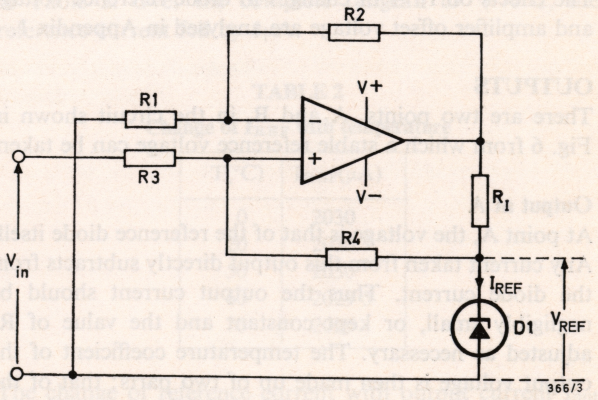

Fig. 3—Resistor R_1 replaced by reference diode

V_{REF} as the control voltage

The reference voltage of the diode is almost independent of temperature and, with the correct resistor values, can be used as a control voltage for the circuit, as shown in Fig. 4. It is seen that R_3 and R_4 are now in parallel and can therefore be replaced by one resistor R_5, as shown in Fig. 5. Although this resistor is not essential, it is retained to reduce the effects of thermal drift on the offset current of the operational amplifier. The value of R_5 should be made equal to R_I in parallel with R_2.

One disadvantage of the circuits discussed so far is that they are bistable. The output voltage, and hence the load current, can be either positive or negative depending on the conditions at switch on. The problem can be resolved by making the negative supply equal to 0V. This is permissible because the amplifier is operating with a common-mode input voltage equal to V_{REF}. The resultant circuit, shown in Fig. 6, requires a single positive power supply only and at switch-on the current is always set in the same sense, with the output voltage positive. For this circuit, Eq. 1 becomes:

$$I_{REF} = \frac{1}{R_I}\cdot\frac{R_2}{R_1}\cdot V_{REF}. \qquad \ldots(2)$$

The output voltage of the amplifier V_o is:

$$V_o = V_{REF}+I_{REF}\,R_I.$$

The smaller the product $I_{REF}\,R_I$ is made, the lower the positive supply to the amplifier can be before the circuit ceases to regulate the current. If $V_{REF}\,R_I$ is made some fraction k of V_{REF}, where $0<k<k_{max}$ (see Appendix 1, Note 1), then

$$I_{REF}R_I = kV_{REF}, \qquad \ldots(3)$$

or

$$R_I = kV_{REF}/I_{REF}.$$

Substituting for $I_{REF}\,R_I$ from Eq. 2 gives:

$$kV_{REF} = \frac{R_2}{R_1}V_{REF},$$

and

$$R_2 = kR_1. \qquad \ldots(4)$$

A suitable value for k is 0·1; that is, the voltage drop across R_I is one tenth of the reference voltage. Thus, the nominal output voltage required of the amplifier is 7·15V. The effects on I_{REF} of changes in diode reference voltage and amplifier offset voltage are analysed in Appendix 1.

OUTPUTS

There are two points, A and B, in the circuit shown in Fig. 6 from which a stable reference voltage can be taken.

Output at A

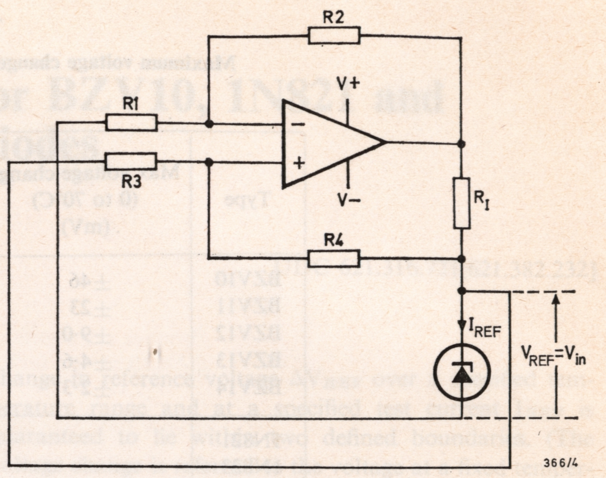

Fig. 4—Input voltage V_{in} replaced by V_{REF}.

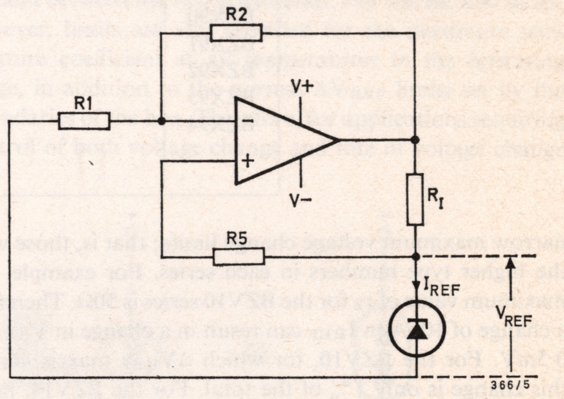

Fig. 5—Resistors R_3 and R_4 replaced by R_5

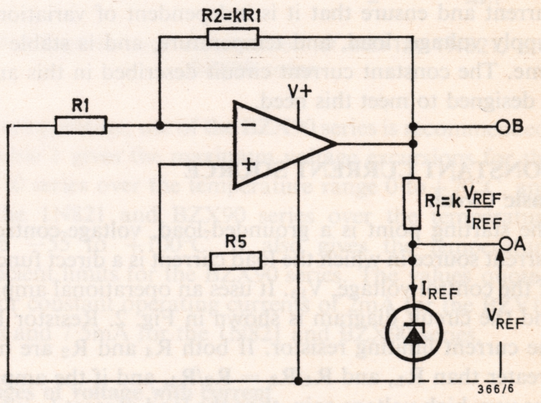

Fig. 6—Circuit with single positive supply

At point A, the voltage is that of the reference diode itself. Any current taken from this output directly subtracts from the diode current. Thus the output current should be negligibly small, or kept constant and the value of R_I adjusted as necessary. The temperature coefficient of the output voltage is then made up of two parts: that of the reference diode, and that of the offset voltage of the operational amplifier. This latter is typically ±7μV/degC, which is one hundredth of the temperature coefficient of the BZV10 and still only one fifth of the temperature coefficient of the BZV14.

If a variable output current is required, it can be obtained by adding another operational amplifier as a voltage follower, as shown in Fig. 7. Again, a single positive power supply is sufficient.

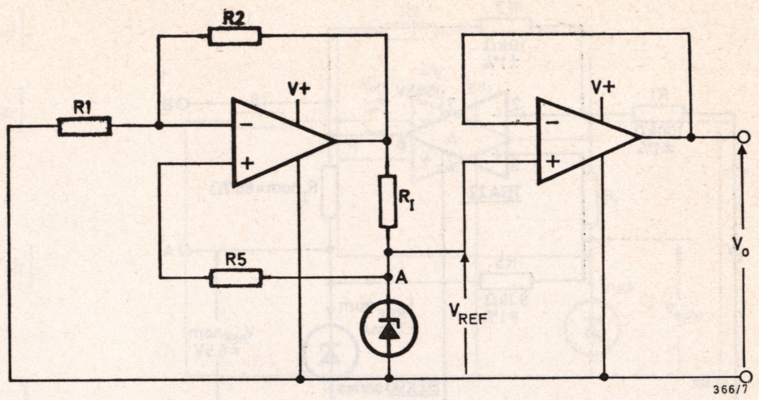

Fig. 7—Circuit with output taken from A through a voltage follower

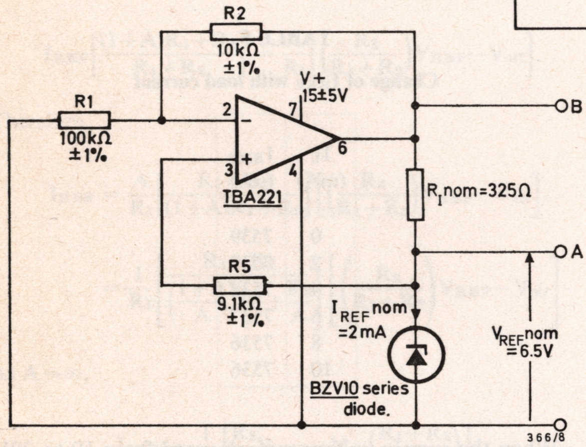

Fig. 8—Practical circuit for BZV10 series

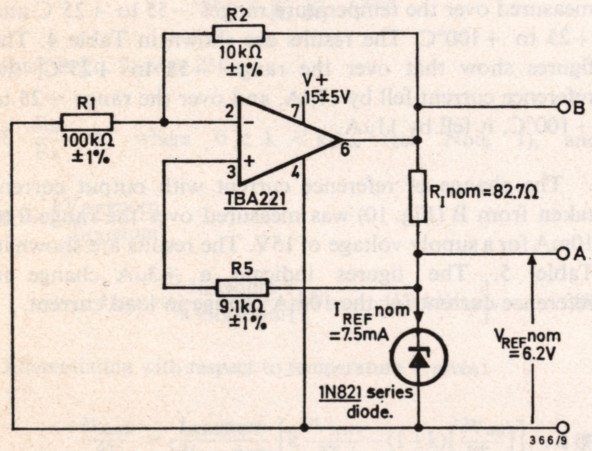

Fig. 9—Practical circuit for 1N821 series

Output at B

At point B, the voltage is $(1+k)V_{REF}$, which for $k = 0{\cdot}1$ is $1{\cdot}1V_{REF}$. Because the current through R_I is kept constant, this output voltage is only slightly less stable than the diode voltage (assuming that R_I is a high stability resistor). Furthermore, output current can be taken from this point without changing the diode current.

By choosing the appropriate value of k, any precisely defined output voltage can be obtained at point B up to a limit set by the ratings of the operational amplifier (see Appendix 1).

PRACTICAL CIRCUITS

The practical circuit for use with the BZV10 series is shown in Fig. 8, that for the 1N821 series in Fig. 9, and that for the BZX90 in Fig. 10. Over the temperature range 0 to +70°C each circuit employs the TBA221 operational amplifier. For temperatures below 0°C and above +70°C, the TBA222 should be used, up to its limits of −55°C and +125°C. All resistors should have a maximum tolerance of ±1%, low temperature coefficients, and good stability with time. Mullard MR30 resistors were used in the laboratory prototypes to obtain the results described in the next section. These have temperature coefficients comparable with those of the diodes. Performance can, of course, be improved if resistors with lower temperature coefficients are used.

Measured results obtained for the circuits of Fig. 8 and Fig. 10 are given below.

Measured performance with BZV13

The performance of the constant current source in Fig. 8 was measured with a BZV13, $V_{REF} = 6{\cdot}64V$, inserted in the circuit. The required value of R_I was thus 332Ω (a 330Ω resistor was used). With the temperature of the diode at 20°C and a supply voltage of 15V, the reference current was 2·030mA, or 2030μA.

When the supply voltage was changed from 10 to 20V, the resultant change in reference current was less than 1μA.

The change of reference current with temperature was measured in the range 0 to +70°C. The results are shown in Table 2. Over the complete range 0 to +70°C, the reference current fell by 1μA.

TABLE 2

Change of I_{REF} with temperature

T(°C)	I_{REF}(μA)
0	2030
20	2030
50	2030
60	2029·5
70	2029

The change of reference current with output current I_{out} taken from point B (Fig. 6) was measured for three supply

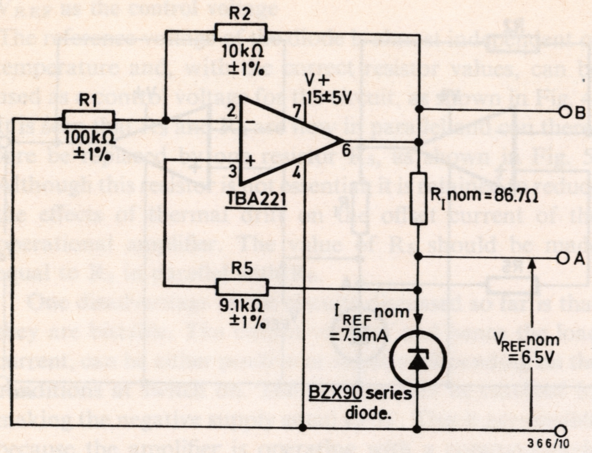

Fig. 10—Practical circuit for BZX90 series

voltages V_s. The results are given in Table 3. With a supply voltage of 20V, and with 0 and 10mA being drawn from point B, the change in reference current just exceeds 1μA. At lower supply voltages, the change was less than 1μA.

TABLE 3

Change of I_{REF} with output current

V_s (V)	I_{out} at B (mA)	I_{REF} (μA)
10	0	2030
10	10	2030
15	0	2030
15	10	2029·2
20	0	2030
20	10	2028·8

Measured performance with BZX93

The performance of the constant current source in Fig. 10 was measured with a BZX93, $V_{REF}=6·312$V, inserted in the circuit. The required value of R_I, 84·5Ω, was made up from 560Ω and 100Ω in parallel. At a temperature of 25°C and with a supply voltage of 15V, the reference current was 7·539mA or 7539μA.

TABLE 4

Change of I_{REF} with temperature

T (°C)	I_{REF} (μA)	T (°C)	I_{REF} (μA)
−55	7556	25	7539
−40	7552	50	7535
−20	7547	75	7531
0	7544	100	7528

TABLE 5

Change of I_{REF} with load current

I_L (mA)	I_{REF} (μA)
0	7539
2	7539
4	7538
6	7537
8	7536
10	7536

When the supply voltage was changed from 10 to 20V, the resultant change in reference current was slightly less than 2μA.

The change of reference current with temperature was measured over the temperature ranges −55 to +25°C and +25 to +100°C. The results are shown in Table 4. The figures show that over the range −55 to +25°C, the reference current fell by 17μA, and over the range +25 to +100°C, it fell by 11μA.

The change of reference current with output current taken from B (Fig. 10) was measured over the range 0 to 10mA for a supply voltage of 15V. The results are shown in Table 5. The figures indicate a ±3μA change in reference current for the 10mA change in load current.

APPENDIX 1

Effects of changes in reference voltage and operational amplifier offset voltage on the reference current

If the offset voltage of the amplifier V_{off} is added to the circuit of Fig. 6 and R_5 is ignored, the circuit becomes that in Fig. 11. If the amplifier voltage gain is −A, then:

$$V_o = V_{REF}+I_{REF}R_I, \qquad \ldots(5)$$

$$V_{REF}+V_i = \frac{R_1}{R_1+R_2}V_o, \qquad \ldots(6)$$

and,

$$V_i+V_{off} = \frac{V_o-V_{REF}}{-A}. \qquad \ldots(7)$$

From Eq. 5:

$$I_{REF} = \frac{V_o-V_{REF}}{R_I}.$$

Substituting for V_o from Eq. 7 gives:

$$I_{REF} = \frac{-A(V_i+V_{off})}{R_I}.$$

Substituting for V_i from Eq. 6 gives:

$$I_{REF} = \frac{-A}{R_I}\left[\left(\frac{R_1}{R_1+R_2}\right)V_o-V_{REF}+V_{off}\right],$$

$$= \frac{-A}{R_I}\left[\left(\frac{R_1}{R_1+R_2}\right)\left(V_{REF}+I_{REF}R_I\right)-V_{REF}+V_{off}\right],$$

$$= \frac{-A}{R_I}\left[\left(\frac{R_1}{R_1+R_2}\right)I_{REF}R_I-\left(\frac{R_2}{R_1+R_2}\right)V_{REF}+V_{off}\right].$$

Therefore,

$$I_{REF}\left[1+A\left(\frac{R_1}{R_1+R_2}\right)\right] = \frac{A}{R_I}\left[\left(\frac{R_2}{R_1+R_2}\right)V_{REF}-V_{off}\right],$$

or,

$$I_{REF}\left[\frac{(1+A)R_1+R_2}{R_1+R_2}\right] = \frac{A}{R_I}\left[\left(\frac{R_2}{R_1+R_2}\right)V_{REF}-V_{off}\right].$$

Therefore,

$$I_{REF} = \frac{A}{R_I}\left[\frac{R_1+R_2}{(1+A)R_1+R_2}\right]\left[\left(\frac{R_2}{R_1+R_2}\right)V_{REF}-V_{off}\right],$$

$$= \frac{1}{R_I}\left[\frac{R_1+R_2}{\left(\frac{1+A}{A}\right)R_1+\frac{R_2}{A}}\right]\left[\left(\frac{R_2}{R_1+R_2}\right)V_{REF}-V_{off}\right].$$

As A→∞,

$$I_{REF}\rightarrow\frac{1}{R_I}\left[\frac{R_2}{R_1}V_{REF}-V_{off}\left(\frac{R_1+R_2}{R_1}\right)\right].$$

If $V_{off} = 0$,

$$I_{REF} = \frac{1}{R_I}\cdot\frac{R_2}{R_1}\cdot V_{REF},$$

which is Eq. 2, page 236.

If $\frac{R_2}{R_1} = k$, where $0 < k < k_{max}$ (see Note 1), and

$$R_I = \frac{kV_{REF}\text{nom}}{I_{REF}\text{nom}},$$

$$I_{REF} = \frac{I_{REF}\text{nom}}{kV_{REF}\text{nom}}\left[kV_{REF}-(1+k)V_{off}\right]. \qquad \ldots(8)$$

Differentiating with respect to temperature T gives:

$$\frac{\partial I_{REF}}{\partial T} = \frac{I_{REF}\text{nom}}{kV_{REF}\text{nom}}\left[k\frac{\partial V_{REF}}{\partial T}-(1+k)\left(\frac{\partial V_{off}}{\partial T}\right)\right]. \qquad \ldots(9)$$

If $\frac{\partial V_{off}}{\partial T} = 0$,

$$\frac{\partial I_{REF}}{\partial T} = \frac{I_{REF}\text{nom}}{V_{REF}\text{nom}}\cdot\frac{\partial V_{REF}}{\partial T}.$$

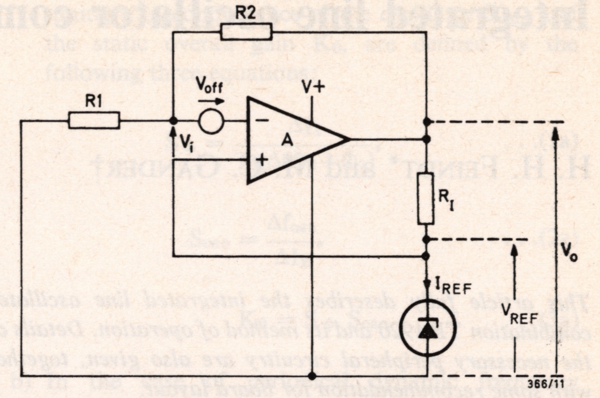

Fig. 11—Equivalent circuit of constant current source with amplifier offset voltage included

For BZV10,

$$\frac{\partial V_{REF}\text{max}}{\partial T} = 6·5\times10^{-4}\text{V/degC},$$

and therefore,

$$\frac{\partial I_{REF}\text{max}}{\partial T} = 2\times10^{-3}\times10^{-4}\text{A/degC}$$
$$= 200\mu\text{A/degC}.$$

For BZV14,

$$\frac{\partial V_{REF}\text{max}}{\partial T} = 6·5\times5\times10^{-6}\text{V/degC},$$

and therefore,

$$\frac{\partial I_{REF}\text{max}}{\partial T} = 2\times10^{-3}\times5\times10^{-6}\text{A/degC},$$
$$= 10\text{nA/degC}.$$

Thus, the smaller the maximum reference voltage change with temperature, the smaller the change in reference current, which is what is required.

If $\frac{\partial V_{REF}}{\partial T} = 0$,

$$\frac{\partial I_{REF}}{\partial T} = \frac{-1}{R_I}\left(\frac{\partial V_{off}}{\partial T}\right)(1+k).$$

Taking $R_I = 325\Omega$, $k = 0·1$, and $\frac{\partial V_{off}}{\partial T} = 7\times10^{-6}$V/degC for the TBA221, then:

$$\frac{\partial I_{REF}}{\partial T} = \frac{1}{325}\times1·1\times7\times10^{-6}\text{A/degC},$$
$$= 24\text{nA/degC}.$$

These changes in reference current are acceptably small,

Note 1

The maximum value of k is determined by the ratings of the operational amplifier.

For the TBA221, $V_{o\,max} = 18$V. Because $V_o = (1+k)V_{REF}$ and $V_{REF}\text{max} = 6·8$V,

$$k_{max} = \frac{18}{6·8}-1$$
$$= 1·65$$

Integrated line oscillator combination TBA920

H. H. Feindt* and M. C. Gander†

UDC 621.3973.32/5

This article fully describes the integrated line oscillator combination TBA920 and its method of operation. Details of the necessary peripheral circuitry are also given, together with some recommendation for board layout.

FUNCTIONS OF LINE OSCILLATOR COMBINATION TBA920

The line oscillator combination TBA920, which contains all the small signal stages for the horizontal deflection of the picture tube, extends the series of monolithic integrated circuits for television receivers marketed by Mullard. This particular circuit is able to perform the following functions (see block diagram, page 242).

a) Sync pulse separation with optional noise inversion.
b) Generation of a line frequency voltage by means of an oscillator, the frequency of which can be current controlled.
c) Phase comparison between sync pulse and the oscillator waveform to generate a control voltage for the automatic tuning of the oscillator to the line frequency and phase position of the sync pulses. Optimum adaptation of the characteristics of this control circuit to the given working conditions (such as pull-in, hold, playback of video recordings on domestic video recorders) by switching of the variable transconductance (flywheel loop gain) and the variable time-constant.
d) Automatic switching of the variable transconductance and the variable time-constant by means of a special phase detector which, with coincidence of sync pulse and line flyback pulse, produces a switching signal which is passed through a Schmitt trigger to achieve noise suppression. These measures make it possible to achieve equally big pull-in and hold ranges for the synchronisation of the oscillator, with good noise suppression and minimum phase deviation.
e) Phase comparison between the oscillator waveform and the middle of the line flyback pulse to generate a control voltage for the correction of switching delay times in the horizontal driving and output stages. This comparison is largely independent of the amplitude, the shape, and the duration of the line flyback pulse. Since in this phase comparison circuit no requirements of noise suppression arise, the circuit can be dimensioned so that even momentary effects, depending for instance on the beam current, can be corrected in the horizontal output stage.
f) Shaping and amplification of the oscillator waveform to obtain pulses for the control of driving stages in horizontal deflection circuits using either transistors or thyristors. The width of the control pulses is adjusted by the voltage arising from phase comparison between the oscillator waveform and line flyback pulse (by displacement of the leading edge of the pulse) in such a way that the switching delay of the subsequent stage is corrected.

The TBA920 also offers the following advantageous characteristics

a) Narrow spread of the phase position between sync pulse and line flyback pulse; also a narrow spread of the unsynchronised oscillator frequency with a specific external circuit.
b) All properties of the circuit are largely independent of temperature and operating voltage
c) Switch-off of the output pulses (which control the horizontal driving and output stage) when the operating voltage drops to one-third of its rated value
d) Protective circuits with internal diodes and external current limiting resistors to protect the IC against pulse loading (h.t. flashover), and short-circuits at all important inputs and outputs.
e) Flexible in application for non-standard requirements.
f) Simple changeover to other horizontal frequencies.

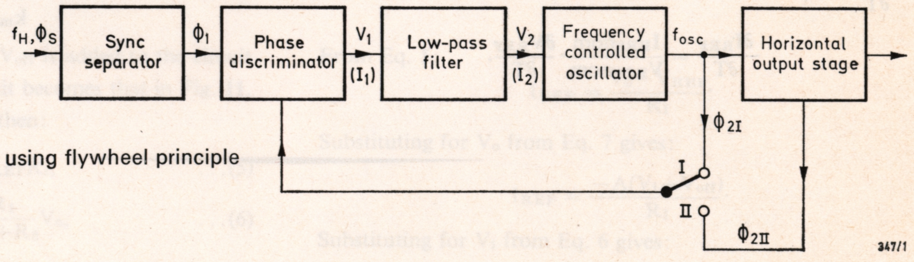

Fig. 1—Horizontal deflection sync using flywheel principle

Basic Functions of the TBA920

Fig. 1 illustrates the main functional blocks in a typical line flywheel synchronising system. Phase comparison can take place either between the sync pulse and a signal derived from the horizontal output stage (generally the line flyback pulse) or between the sync pulse and a signal taken from the oscillator.

With phase comparison between the separated sync pulse and the line flyback pulse the various phase shifts in the oscillator, line driver circuit and horizontal output stage are all compensated automatically. A well known disadvantage in this method, however, is that the amplitude, shape and duration of the line flyback pulse are dependent upon picture tube beam current variations and, in colour receivers, the action of raster shape correction circuits. Consequently the dimensioning of the low-pass filter cannot be the optimum for securing good synchronising noise immunity but a poor compromise has to be found between this and the rejection of the effects of the distortions on the line flyback pulse. If, however, phase comparison between sync pulse and oscillator signal is used, the controlled phase position is independent of the amplitude, shape, and duration of the line flyback pulse. The difficulty then is that static and dynamic changes in the switching times of the output stage may now appear, and will require further measures for correction.

Clearly, the familiar, simple circuits for flywheel synchronisation are unable to provide a fully satisfactory solution, because contradictory requirements have to be met. However, by incorporating a further phase control loop the oscillator-to-sync and horizontal output-to-oscillator phase lock requirements may each be dealt with separately. The additional loop is incorporated into the TBA920 and will be described fully below.

The following general objectives are aimed at with a flywheel system such as that embodied in the TBA920:

1) Optimum holding behaviour; that is, the least possible phase difference in the synchronised state, so that only negligible shifts occur between picture and scan. This requirement should be met in the following conditions:

   a) With a static frequency Δf between sync pulse frequency f_H (line frequency) and unsynchronised oscillator frequency f_{osc}. This can be achieved by a large overall gain K_0 in the control circuit (loop gain). At low frequencies K_0 is practically equal to the product of the static transconductance of the phase discriminator, given by

   $$S_{\phi}' = \frac{\Delta V_1}{\Delta_{(\phi 2 - \phi 1)}}, \qquad \ldots(1)$$

   and the static tuning transconductance of the oscillator, given by

   $$S_{osc}' = \frac{\Delta f_{osc}}{\Delta V_2}, \qquad \ldots(2)$$

   that is,

   $$K_0' = S_{\phi}'.S_{osc}'. \qquad \ldots(3)$$

   Instead of the voltages V_1 and V_2, corresponding currents I_1 and I_2 can be used, and the phase difference $\Delta(\Phi_2 - \Phi_1)$ can be replaced by the time difference $\Delta T = T_H \Delta(\Phi_2 - \Phi_1)$, where T_H is the duration of the line period. In that case the static transconductance of the discriminator S_{ϕ}, the static tuning transconductance of the oscillator S_{osc}, and the static overall gain K_0, are defined by the following three equations:

   $$S_{\phi} = \frac{\Delta I_1}{T_H \Delta(\Phi_2 - \Phi_1)}, \qquad \ldots(1a)$$

   $$S_{osc} = \frac{\Delta f_{osc}}{\Delta I_2}, \qquad \ldots(2a)$$

   $$K_0 = S_{\phi}.\ S_{osc}. \qquad \ldots(3a)$$

   b) In the case of periodical dynamic frequency variations Δf, that is, in the case of line frequency modulation, for example. In order to avoid resonance magnification, the overall gain K_0 and the filtering effect of the low-pass filter should not be made too great.

   c) Under the influence of interference, particularly noise. An appropriate standard with which to describe the effect of such additive interference is the noise bandwidth, which should be as small as possible. In order to achieve this, a small overall gain K_0 and a strong filtering effect of the low-pass filter are required. The low-pass filter should be made up of at least two CR components.

2) Optimum capturing behaviour. This implies:

   a) Short pull-in time, that is, a short correction time, so that the oscillator, after prolonged interference or phase jumps of the sync signal, can be pulled in quickly again (specially important for picture reproduction with domestic video recorders). This requires a large overall gain K_0 and a small filtering effect of the low-pass network.

   b) A pull-in range adapted to the tolerances of the oscillator and sync pulse frequency. A pull-in range greater than that chosen in accordance with these considerations is not necessary and can be a disadvantage. By limitation of the oscillator control range it is possible to limit the pull-in range (and also the holding range).

In the case of colour television receivers, further considerations must be added to the above:

   c) The phase comparison must be largely independent of the amplitude, width and shape of the line flyback pulse. These properties of the line flyback pulse are influenced by the beam current, the raster correction, the h.t. regulation, and by component tolerances.

   d) The phase difference ΔΦ must be specially small, because derivatives of the line flyback pulse are used for burst gating and black level clamping where accurate timing is important.

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Fig. 2, which represents the block diagram of the TBA920 in simplified form, shows at the bottom the first control loop, consisting of the phase discriminator 1, the filter 1, and the oscillator; this loop brings about the synchronisation of the oscillator to the sync pulses. In the phase discriminator 1 the phase Φ_{11} of the separated sync pulses is compared with the oscillator phase Φ_{12}. The control loop can be designed for favourable pull-in and holding performance, without any need to consider the output stage effects. The oscillator then controls the output stage of the horizontal deflection via a phase shifter, the phase shift of which can be set by means of a voltage. A second control loop, consisting of the phase discriminator 2, the filter 2, the controlled phase shifter, and the horizontal output stage, compensates the output stage effects. Because this control loop no longer has to meet any requirements in respect of the elimination of noise and interference, a large loop gain and a short time-constant do not incur any penalty, therefore very rapid correction of the output stage effects can be achieved.

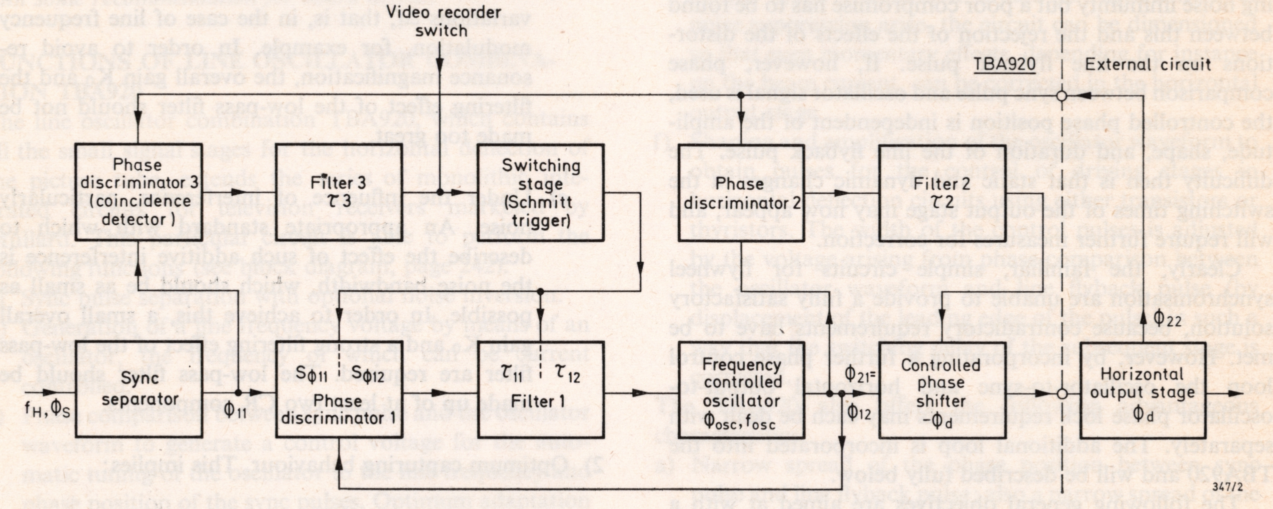
Video recorder switch
TBA920
External circuit
Phase discriminator 3 (coincidence detector)
Filter 3 τ3
Switching stage (Schmitt trigger)
Phase discriminator 2
Filter 2 τ2
Φ22
f_H, Φ_S
Sync separator
Φ11
SΦ11 SΦ12
Phase discriminator 1
τ11 τ12
Filter 1
Frequency controlled oscillator Φosc, fosc
Φ21=
Φ12
Controlled phase shifter −Φd
Horizontal output stage Φd
347/2

Fig. 2—Simplified block diagram of the TBA920

The contradictory demands in respect of the pull-in and holding range of the first control loop can largely be met by varying the slope of the phase discriminator 1 (and thus of the overall gain K_0) and of the filtering effect of the filter 1. If the oscillator is not synchronised, then for reliable and rapid pull-in the large discriminator slope $S_{\phi 12}$ and the short-time constant τ_{12} for reduced filtering effect are switched in. Once the process of pull-in is ended, and the oscillator is synchronised, switching over to the smaller discriminator slope $S_{\phi 11}$ and the time-constant τ_{11} for greater filtering takes place, in order to achieve good interference immunity in the holding state. The choice of $S_{\phi 11}$ and τ_{11} can then be determined by the same considerations as in the conventional circuits.

In the TBA920 this switching over is performed automatically by means of a special phase discriminator, shown at the top-left in Fig. 2 and working as a coincidence detector. This discriminator, in which the phase position Φ_{11} of the processed sync pulse is compared with the phase position Φ_{22} of the line flyback pulse, supplies a voltage only if the line flyback pulse and the sync pulse show adequate overlapping. The resulting switching voltage triggers the switching over of the phase discriminator 1 and the filter 1 described above. To eliminate interference in the switching voltage originating in the coincidence detector, a third low-pass filter and a Schmitt trigger are used, the hysteresis of the Schmitt trigger preventing erratic switching resulting from interference in the input signal. The time-constant τ_3 of the third filter determines the time elapsing between the end of the pull-in process and the switching over of the slope and of the time-constant: thus rapid pull-in occurs when a signal is found, and then noise and interference suppression follow after a short delay.

The automatic switching over can be blocked by an external switch, with which the steep slope $S_{\phi 12}$ of the discriminator and the time-constant τ_{12} for slight filtering effect can be switched in. This is necessary during reproduction with a domestic video recorder. In this case, because of deviations in the velocity of the tape and fluctuations in the synchronisation, much bigger static and dynamic departures of the line frequency from the standard value must be expected, than with a broadcast programme. Furthermore, phase jumps of up to ±20µs may occur in the vertical interval, which must have been corrected before the beginning of the visible picture (after about 20 to 30 lines). For these reasons the control loop 1 must always be switched to a large gain K_0 and to a short correction time during playback with domestic video recorders.

Circuit Description, and general application considerations

Fig. 3 shows the detailed block diagram of the TBA920 with a simplified external circuit.

The input terminal 8 of the sync pulse separator stage receives the combined video and sync signal (with positive-going sync pulses) via a CR network. At terminal 7 the sync signal, separated from the video signal, is then available at a low-impedance output. An optional impulsive noise gating facility is provided at pin 9. The use of this would be necessary only in cases where the applied video signal had not already been noise-cancelled. The sync signal appearing at terminal 7 is passed via a suitable CR network to the vertical deflection stage and also to terminal 6 via a network which is essentially a differentiating circuit.

The voltage appearing at terminal 6 is used for synchronising the line oscillator, which is effected by means of the control loop 1 (Fig. 2). The frequency f_{osc} of the controlled-frequency oscillator depends on the external capacitance $C_{14-16} = C_{osc}$, the external adjustable resistance $R_{15-16} = R_{osc}$, and the current fed (additionally) into terminal 15. In the phase discriminator 1 the phase position of the oscillator is now compared with the phase position of the processed sync pulse at terminal 6, and a pulsed control current i_{12}, corresponding to the phase difference of these two signals and limited to a maximum amplitude, is made available at terminal 12. With the external filter 1, consisting of CR components and connected between terminals 11, 12, and earth, the control current i_{12} is filtered and subsequently passed to the oscillator (terminal 15) to control its frequency.

The switching of the slope of phase discriminator 1 and the filter time-constant is carried out by a Schmitt trigger circuit driven by a coincidence detector. The coincidence detector (phase discriminator 3 in Fig. 2) supplies a control voltage only if the sync pulses appearing at terminal 7 sufficiently overlap the line flyback pulses applied to terminal 5 (via an integrating or differentiating circuit). For the filtering of this control voltage an external CR network (in Fig. 2, filter 3 with time-constant τ_3) is provided at terminal 10. Inactivation of the automatic switching and switching-in of the steeper discriminator slope and smaller filtering effect of filter 1, can be achieved by switching terminal 10 to earth; this could be used, for example in video recorder operation. Below a certain minimum l.t. supply voltage V_B min, a steep slope of the phase discriminator 1 and a slight filtering effect of filter 1 will always be switched in, this is represented symbolically in the block diagram by a switch $f(V_B)$.

The oscillator waveform is passed to a pulse shaping stage, which also operates as a controlled phase-shifter: the phase position of the lagging edge remains fixed, but the

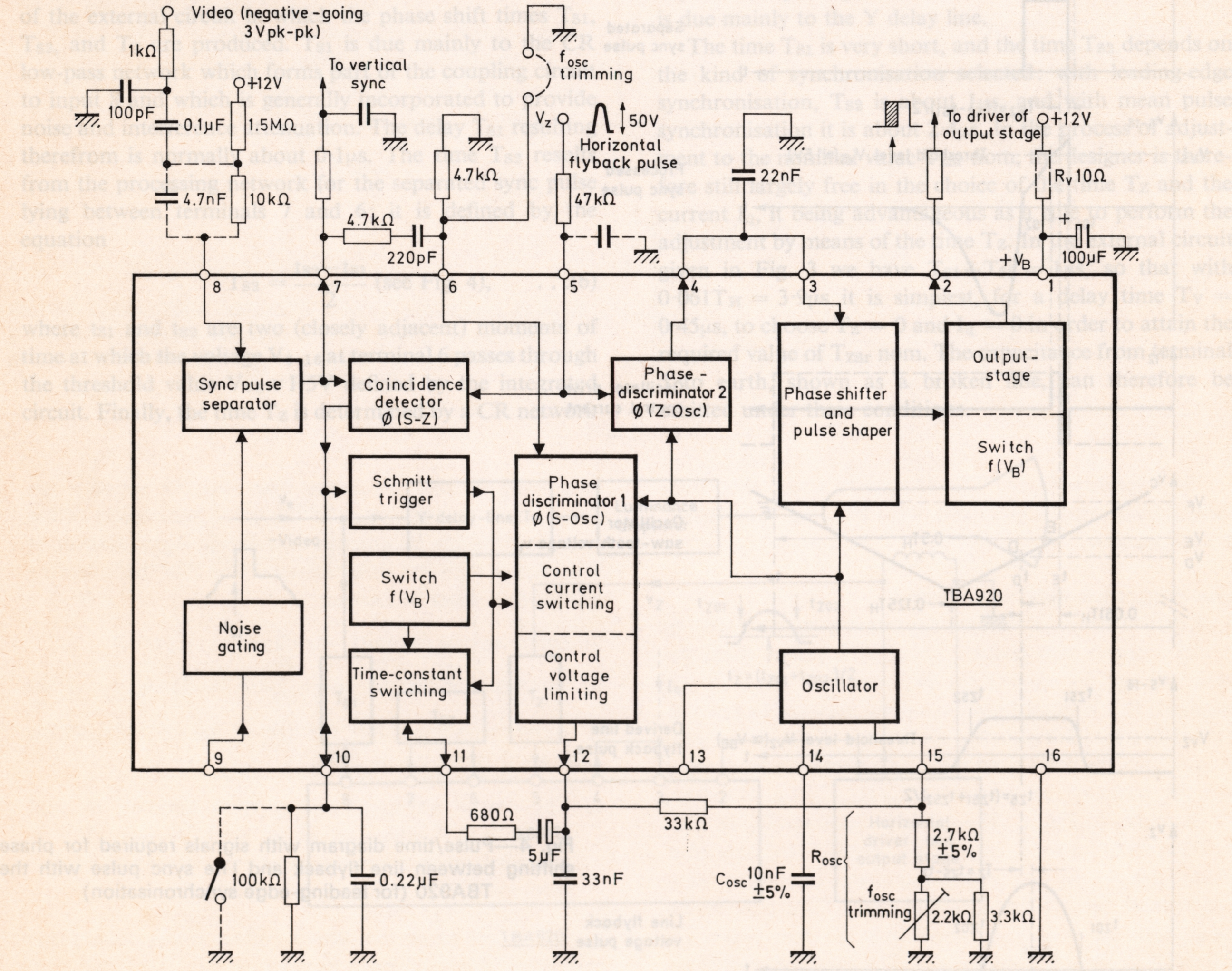
Video (negative-going 3Vpk-pk)
1kΩ
100pF
0.1µF
+12V
1.5MΩ
4.7nF
10kΩ
To vertical sync
4.7kΩ
220pF
4.7kΩ
fosc trimming
Vz
50V
Horizontal flyback pulse
47kΩ
22nF
To driver of output stage
+12V
Rv 10Ω
+VB
100µF
8
7
6
5
4
3
2
1
Sync pulse separator
Coincidence detector Ø(S-Z)
Phase-discriminator 2 Ø(Z-Osc)
Phase shifter and pulse shaper
Output-stage
Switch f(VB)
Schmitt trigger
Phase discriminator 1 Ø(S-Osc)
Switch f(VB)
Control current switching
Noise gating
Time-constant switching
Control voltage limiting
TBA920
Oscillator
9
10
11
12
13
14
15
16
680Ω
5µF
33kΩ
100kΩ
0.22µF
33nF
Cosc 10nF ±5%
Rosc
2.7kΩ ±5%
fosc trimming
2.2kΩ
3.3kΩ
347/3

Fig. 3—Detailed block diagram of the TBA920 with a typical simple external network

position of the leading edge, and hence also the width of the shaped square-wave pulses, depends on the voltage at the input terminal 3. The shaped square-wave pulses which are available in amplified form at output terminal 2 can therefore drive the line output stage whose phase position is adjusted at terminal 3. To ensure that the phase position of the deflection does not depend on delay times in the line output stage, the phase position of the drive pulses is adjusted automatically by means of a control voltage supplied by the phase discriminator 2, in which the phase position of the line flyback pulse at terminal 5 is compared with the position of the oscillator waveform. This control current, which appears at terminal 4, is filtered and passed to terminal 3. At a certain minimum l.t. supply voltage the output stage is blocked by a switch indicated in Fig. 3 by $f(V)_B$, which stops any further driving of the output stage.

Phasing of Line Flyback Pulse with Reference to Sync Pulse

As is clear from the foregoing description the line oscillator must act as the phase determining element of a pulse shaping stage and two phase discriminators. The oscillator is a triangle generator with linearly rising and falling signal voltage, achieved by means of a current source circuit, a threshold switch and two threshold values, a reversing switch, and a current inverter. This principle, particularly because of the linearity of the delta voltage generated, is suitable for the determination of different phase positions, with very little spread, by means of voltage comparators.

Before the individual circuit components are considered in more detail, it is necessary first of all to define the phase positions of certain important signals and to discuss their relationships. These signals have, to facilitate explanation, been grouped together in a diagram (Fig. 4), their leading edges being in phase.

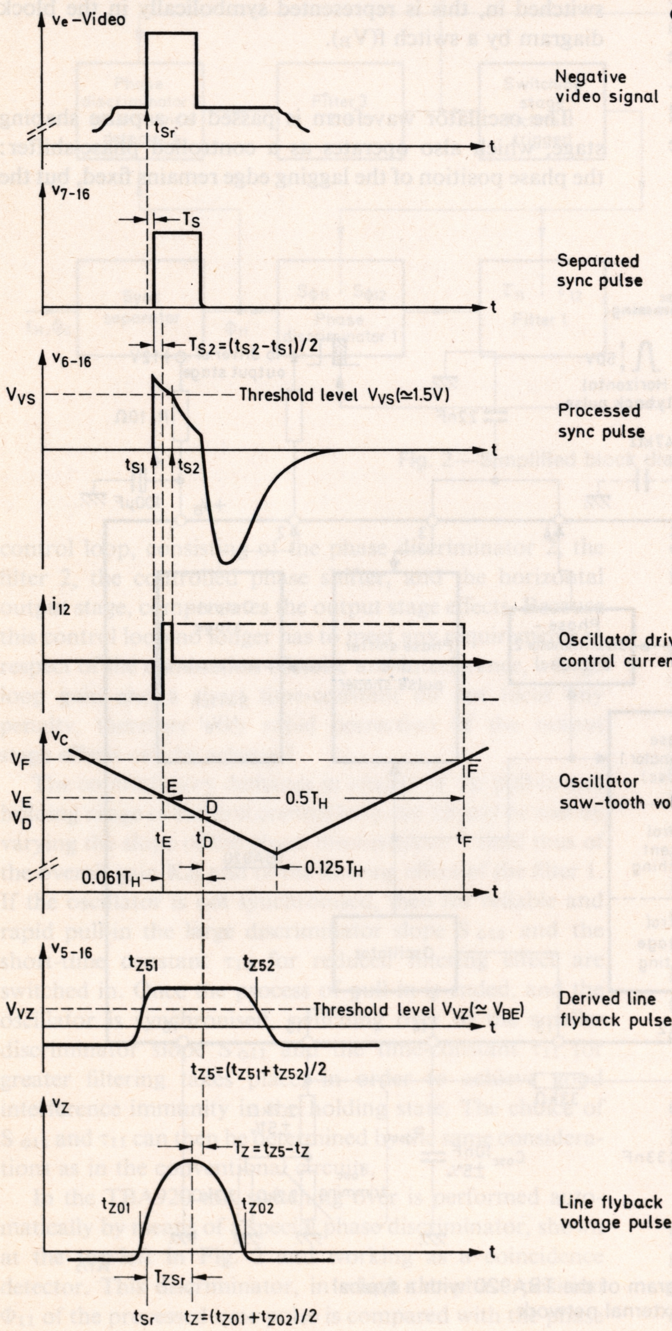

Fig. 4—Pulse/time diagram with signals required for phase shifting between line flyback and line sync pulse with the TBA920 (for leading-edge synchronisation)

The position of the sync pulse is determined, as mentioned above, by the time t_{Sr} of its leading edge. The phase position of the line flyback pulse, however, is defined by the time of its mid-point, that is, by the arithmetic mean

$$t_Z = \frac{t_{Z01}+t_{Z02}}{2} \qquad \ldots(4)$$

where t_{Z01} and t_{Z02} are those instants of the flyback at which the line flyback voltage V_Z just passes through zero. These two instants correspond almost exactly with the points of reversal of the horizontal deflection.

The difference between the moments t_{Sr} and t_Z, that is, the phase position T_{ZSr} of the line flyback pulse in relation to the sync pulse (expressed in terms of the time scale) is given, on the basis of the above definitions, by

$$t_Z - t_{Sr} = T_{ZSr} = 0{\cdot}061\,T_H + T_{S1} + T_{S2} - T_Z - qI_q \qquad \ldots(5)$$

The first term on the right-hand side of Eq. 5, in which T_H represents the duration of a line, is defined by the integrated circuit while the other three terms result from the external circuit and from a current I_q additionally fed externally to the terminal 3 (and 4); the constant q is about 45μs/mA.

The block diagram shown in Fig. 5 indicates the parts of the external circuit in which the phase shift times T_{S1}, T_{S2}, and T_Z are produced. T_{S1} is due mainly to the CR low-pass network which forms part of the coupling circuit to input 8 and which is generally incorporated to provide noise and interference attenuation. The delay T_{S1} resulting therefrom is normally about 0·1μs. The time T_{S2} results from the processing network for the separated sync pulse lying between terminals 7 and 6; it is defined by the equation

$$T_{S2} = \frac{t_{S2}-t_{S1}}{2} \text{ (see Fig. 4),} \qquad \ldots(6)$$

where t_{S1} and t_{S2} are two (closely adjacent) moments of time at which the voltage V_{6-16} at terminal 6 passes through the threshold value $V_{VS} \approx 1{\cdot}5V$ defined by the integrated circuit. Finally, the time T_Z is determined by a CR network in series with terminal 5; as a rough approximation T_Z is the difference between the middle of the pulse occurring at terminal 5 and the middle of the line flyback pulse.

The exact definition is

$$T_Z = t_{Z5} - t_Z, \qquad \ldots(7)$$

in which the time t_Z is given by Eq. 4 and time t_{Z5} is defined by the equation

$$t_{Z5} = \frac{t_{Z51}+t_{Z52}}{2}. \qquad \ldots(8)$$

t_{Z51} and t_{Z52} are the instants during a flyback at which the voltage V_{5-16} at terminal 5 just passes through the threshold value $V_{VZ}(\approx V_{BE})$ defined by the integrated circuit. Because of the condition

$$|T_Z| \leqslant T_H/2 \qquad \ldots(7a)$$

the ambiguity inherent in defining the relationship Eq. 7 is eliminated. Depending on whether T_Z is to be positive (trailing) or negative (leading), an integrating or a differentiating network must be connected in series with terminal 5.

With the current U.K. television standard the nominal value of the phase shift time between line flyback and sync pulse is

$$T_{ZSr}\text{ nom} = 4{\cdot}475\mu s + T_V, \qquad \ldots(9)$$

where T_V is the delay time occurring in the video amplifier beyond the sync signal take-off, which, in colour receivers, is due mainly to the Y delay line.

The time T_{S1} is very short, and the time T_{S2} depends on the kind of synchronisation selected: with leading-edge synchronisation, T_{S2} is about 1μs, and with mean pulse synchronisation it is about 2·4μs. In the process of adjustment to the nominal value T_{ZSr} nom, the designer is therefore still largely free in the choice of the time T_Z and the current I_q, it being advantageous as a rule to perform the adjustment by means of the time T_Z. In the external circuit given in Fig. 3 we have $T_{S1}+T_{S2} = 1\mu s$, so that with $0{\cdot}061T_H = 3{\cdot}9\mu s$ it is simplest, for a delay time $T_V = 0{\cdot}45\mu s$, to choose $T_Z = 0$ and $I_q = 0$ in order to attain the required value of T_{ZSr} nom. The capacitance from terminal 5 to earth, shown as a broken line, can therefore be omitted under these conditions.

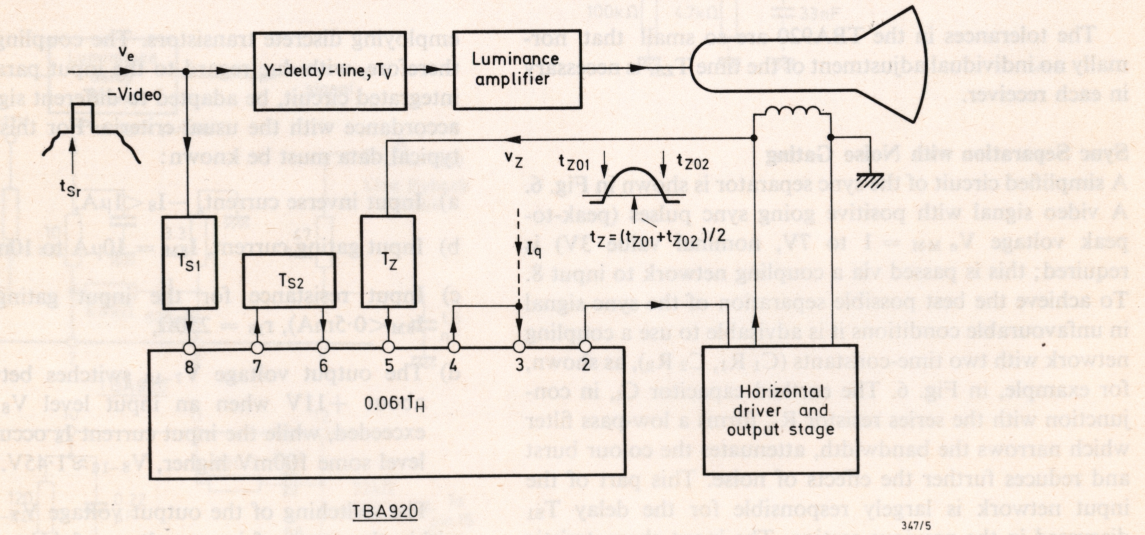

Fig. 5—Block diagram showing the external signal flow and the position of the delaying or phase-lead networks

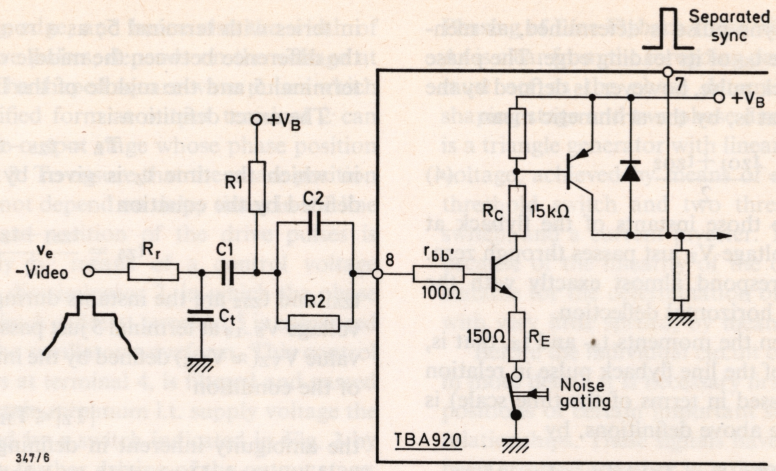

Fig. 6—Basic circuit diagram of pulse separation stage with a coupling network having two time-constants at the input

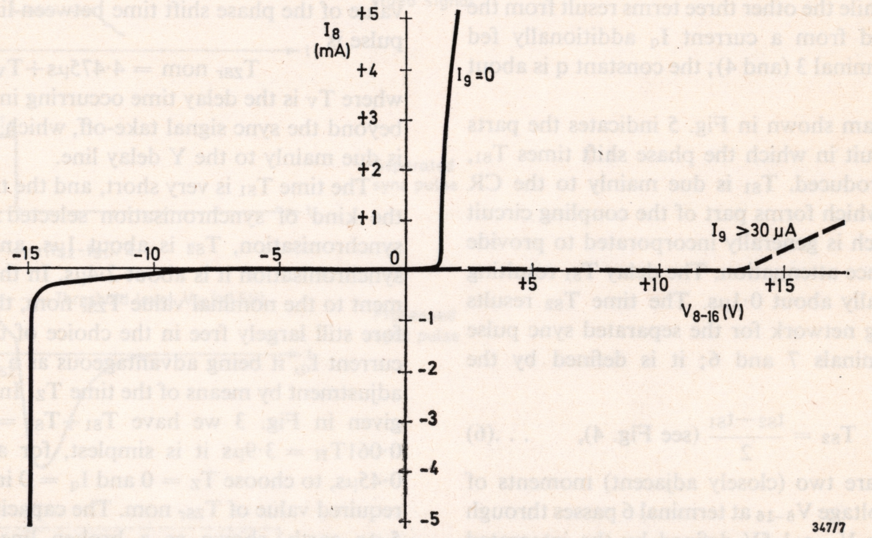

Fig. 7—Input characteristic I_8 versus $V_{8\text{-}16}$ of the TBA920 at terminal 8

The tolerances in the TBA920 are so small that normally no individual adjustment of the time T_{ZSr} is necessary in each receiver.

Sync Separation with Noise Gating

A simplified circuit of the sync separator is shown in Fig. 6. A video signal with positive going sync pulses (peak-to-peak voltage $V_{e\,MM} = 1$ to 7V, nominal value 3V) is required; this is passed via a coupling network to input 8. To achieve the best possible separation of the sync signal in unfavourable conditions it is advisable to use a coupling network with two time-constants ($C_1\,R_1$, $C_2\,R_2$), as shown, for example, in Fig. 6. The earthed capacitor C_t, in conjunction with the series resistor R_r, forms a low-pass filter which narrows the bandwidth, attenuates the colour burst and reduces further the effects of noise. This part of the input network is largely responsible for the delay T_{S1} discussed in the previous section. The input characteristic of the circuit at terminal 8 is represented in Fig. 7. It corresponds quite closely to that of separator stages employing discrete transistors. The coupling network can therefore, with due regard to the input parameters of the integrated circuit, be adapted to different signal sources in accordance with the usual criteria. For this the following typical data must be known:

a) Input inverse current, $-I_8 < 1\mu A$,

b) Input gating current, $I_{8M} = 10\mu A$ to 10mA,

c) Input resistance for the input gating current (at $I_{8M} < 0{\cdot}5mA$), $r_{i8} = 250\Omega$,

d) The output voltage V_{7-16} switches between 0V and about +11V when an input level $V_{8-16} \approx 1{\cdot}35V$ is exceeded, while the input current I_8 occurs at an input level some 100mV higher, $V_{8-16} \approx 1{\cdot}45V$.

The switching of the output voltage V_{7-16} takes place within the range of input voltage of $\Delta V_{8-16} \approx 10mA$ and within a range of input current of $\Delta I_8 \approx 0{\cdot}1\mu V$. The input characteristic for terminal 8 is illustrated in Fig. 7.

The circuits of Fig. 3 and Fig. 8 show the values of coupling networks which have been used in practice. In the capacitive coupling used, the cut-off bias is determined largely automatically through the charging of the capacitors C_1 and C_2, so that fluctuations of the video signal do not cause disturbances.

Complete protection of the pulse separator stage against extremely heavy noise at input 8 (with e.h.t. flashovers, for example) is not possible in semiconductor practice. If the input video signal is carried on a long lead, useful protection can be achieved by the use of a screened lead, the screening being earthed at both ends if possible.

Noise gating is possible by means of positive pulses at terminal 9 which, when they exceed a threshold value of $V_{9-16} \approx 0{\cdot}6V \approx V_{BE}$, result in current pulses $I_9 > 30\mu A$. The action of the noise gating stage can be seen from the schematic diagram of Fig. 6. If signals occur at terminal 9 exceeding the given threshold value, the switch opens and the voltage V_{7-16}, irrespective of the input value V_{8-16}, remains at the level of 0V. The blanking of noise signals requires signals at terminal 9 which consist of the noise pulses separated from the rest of the signal. Because the sync separator and the noise gate both require input signals of the same polarity, no reversing stage is needed for the generation of the gating pulse.

An example of a noise pulse separation circuit as shown in Fig. 8. The clipping level adjusts itself automatically.

The separated sync pulses, protected from interference, are available at the emitter follower output, terminal 7. With a rising or high output level, the output resistance r_{i7} is very low, but with an output voltage $V_{7-16} \approx 0V$, $r_{i7} \approx 2{\cdot}2k\Omega$.

At terminal 7 it is possible to connect an integration network of relatively low resistance ($R > 2{\cdot}2k\Omega$) for the formation of the vertical sync pulses. In the event of direct short-circuiting between terminals 7 and 16 (earth) there is a risk of damage. Current limitation can be achieved by an external protective resistance (possibly part of the vertical integration network), which is connected directly to terminal 7.

For the shaping of the line sync pulse, an external network is connected between terminals 7 and 6. Essentially its function is to effect a voltage division and a differentiation. To improve immunity to interference it is possible to attenuate to some extent h.f. components by an additional grounded capacitance. The dimensioning of the shaping network depends on the kind of synchronisation desired. Fig. 3 and 8 show examples of a network appropriate for leading-edge synchronisation and Fig. 9 illustrates that for mean-pulse synchronisation. The remaining external network must, in accordance with Eqs. 5 and 9, be adapted to the delay $T_{S1} + T_{S2}$, which itself depends on the

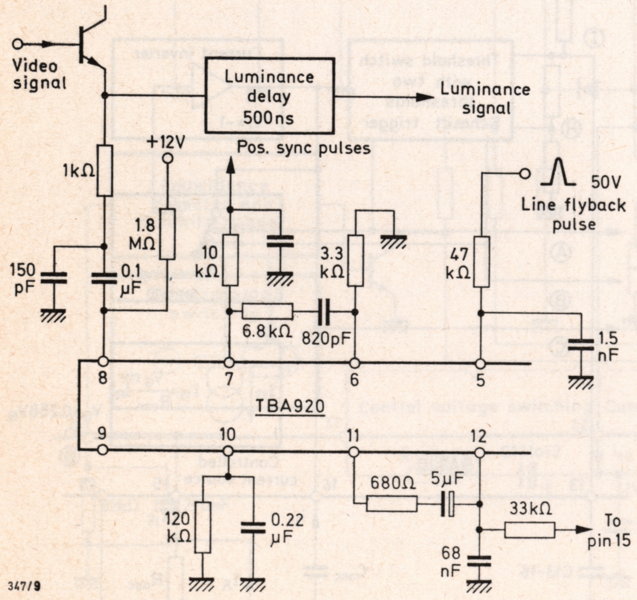

Fig. 8—Dimensioned example of a coupling network at input 8 of the sync signal separation stage and of a network for generating blanking pulses of adequate amplitude for noise blanking at terminal 9

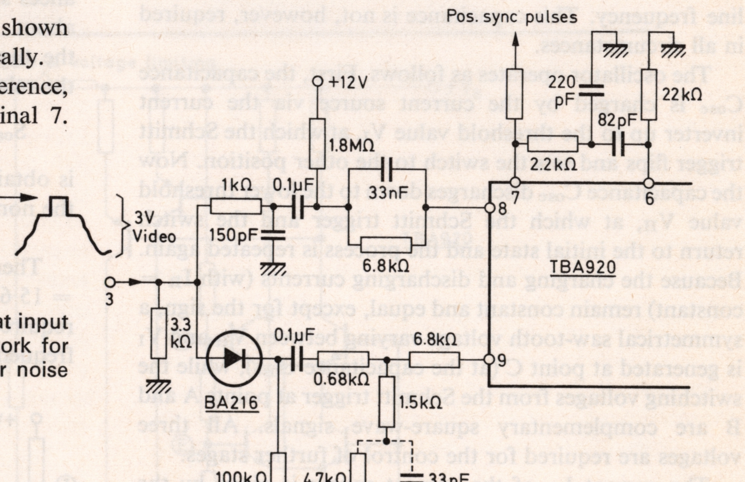

Fig. 9—Dimensioned example of the external network of TBA920 with mean-pulse synchronisation

video signal input network at terminal 8, on the sync pulse shaping network, at terminal 7 and on the threshold level of the phase discriminator 1 (oscillator sync pulse at terminal 6). This is true particularly of the networks which determine the time T_Z and the current I_q, but it applies also to the time-constant τ_3 of the coincidence detector filter at terminal 10. Examples of networks appropriate to leading-edge synchronisations and meanpulse synchronisation are shown in Fig. 3 and Fig. 9.

Oscillator and Phase Discriminator 1

A suitable low-inertia oscillator can be designed in which the frequency is determined by alternately charging and discharging a capacitor. Such an oscillator is shown in Fig. 10 and consists of a current generator (whose current I_{15} depends on the network at terminal 15 and on the control current I_R), a reversing switch, a current inverter, and a Schmitt trigger which controls the switch (and of which the two switching thresholds V_H and V_I are determined by an internal voltage divider connected to the supply voltage), and also an external capacitance $C_{14-16} = C_{osc}$ and an external resistance $R_{15-16} = R_{osc}$. The reference voltage $V_I = (2/3)\ V_B$ can be filtered by an external capacitance C_{13-16} at terminal 13 and thus freed from disturbances at line frequency. This capacitance is not, however, required in all circumstances.

The oscillator operates as follows. First, the capacitance C_{osc} is charged by the current source via the current inverter up to the threshold value V_I, at which the Schmitt trigger flips and sets the switch to the other position. Now the capacitance C_{osc} discharges down to the lower threshold value V_H, at which the Schmitt trigger and the switch return to the initial state and the process is repeated again. Because the charging and discharging currents (with I_R = constant) remain constant and equal, except for the sign, a symmetrical saw-tooth voltage varying between V_H and V_I is generated at point C (at the capacitance C_{osc}), while the switching voltages from the Schmitt trigger at points A and B are complementary square-wave signals. All three voltages are required for the control of further stages.

The current I_{15} of the current source is given by the relationship

$$I_{15} = \frac{V_G}{R_{osc}} - I_R, \qquad \ldots(10)$$

in which

$$V_G = V_{15-16} = 0{\cdot}258V_B, \text{ and } V_{G\,nom} = 3{\cdot}1V \qquad \ldots(11)$$

and I_R is the control current originating in the phase comparison between the oscillator and the sync signal. Remembering that

$$V_I - V_H = 0{\cdot}25V_B, \qquad \ldots(12)$$

then, from the above, the frequency of the oscillator is given by

$$f_{osc} = \frac{I_{15}}{2\,C_{osc}(V_I - V_H)} = \frac{V_G}{2\,R_{osc}\,C_{osc}(V_I - V_H)}$$
$$= \frac{I_R}{2\,C_{osc}(V_I - V_H)}, \qquad \ldots(13)$$

while the frequency of the uncontrolled ($I_R = 0$), free-running oscillator is given by

$$f_{osc\,0} = \frac{V_G}{2\,R_{osc}\,C_{osc}(V_I - V_H)} = \frac{K_1}{R_{osc}\,C_{osc}}, \qquad \ldots(13a)$$

in which the constant K_1 is practically independent of the supply voltage V_B and in the nominal case $K_{1\,nom} = 0{\cdot}516$. With $C_{osc} = 0$ the maximum frequency determined by the switching is about 1·5MHz. The free oscillator frequency $f_{osc\,0}$ can thus be chosen within wide limits by means of the external components C_{osc} and R_{osc}. For the frequency-determining capacitance C_{osc} a high-quality capacitor of close tolerance (±2%) and low temperature coefficient should be used. To keep the effect of switching capacitances small, the capacitance C_{osc} should not be less than about 10nF. This capacitance furthermore determines the tuning steepness S_{osc} of the oscillator. From Eq. 13 the relationship

$$S_{osc} = \frac{d\,f_{osc}}{d\,I_{15}} = \frac{1}{2C_{osc}\,(V_I - V_H)} = \frac{2}{C_{osc}V_B} \qquad \ldots(14)$$

is obtained. With the values $V_B = 12V$ and $C_{osc} = 10nF$ the nominal slope becomes

$$S_{osc\,nom} = 16{\cdot}7\text{Hz}/\mu\text{A}.$$

Therefore to achieve an oscillator frequency $f_{osc\,0} = f_H = 15{\cdot}625$kHz, an oscillator resistance $R_{osc} = 3{\cdot}3$kΩ is required at $C_{osc} = 10$nF. For setting of the oscillator frequency it is possible either to make the resistance R_{osc} adjustable or to feed a current into terminal 15 via a potentiometer circuit. Practical network suggestions are shown in Figs. 3 and 11.

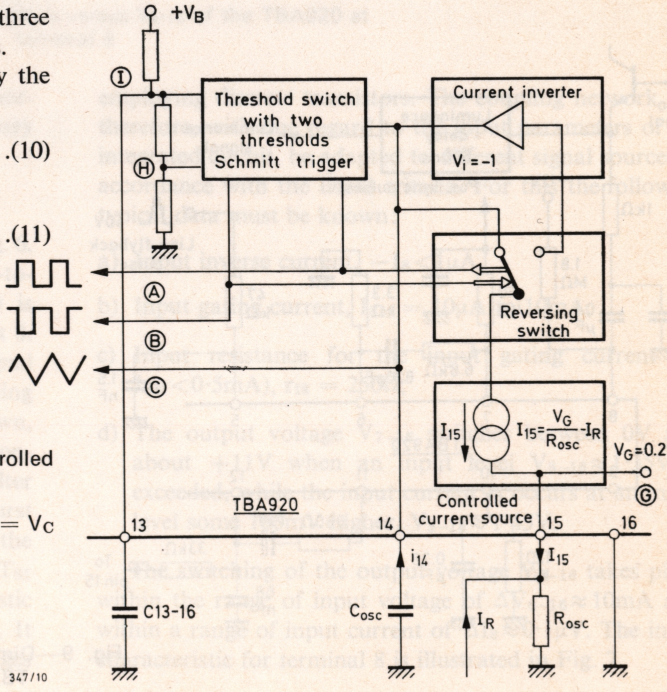

Fig. 10—Basic circuit diagram of the frequency controlled oscillator in the TBA920

$V_{15-16} = V_G = 0{\cdot}258\ V_B;\ V_I - V_H = 0{\cdot}25\ V_B;\ V_{14-16} = V_C$

With $R_3 = \infty$ and $I_R = 0$ in the network used in Fig. 11 for the trimming of the free oscillator frequency, one obtains

$$f_{osc\,0} = \frac{K_1}{C_{osc}}\left[\frac{R_1 + R_{21} + R_{22}}{R_1(R_{21} + R_{22})} - \frac{K_2}{R_{21} + R_{22}}\right] \qquad \ldots(15)$$

where $K_{2\,nom} = 3{\cdot}88$. With this network, a trimming range of ±15% is obtained with a resistance $R_3 = 15$kΩ and a trimming range of ±10% with $R_3 = 27$kΩ.

In multistandard receivers, other line frequencies can be obtained by switching of C_{osc} or R_{osc}. If C_{osc} is switched, the relative values of the frequency adjustment range, the control slope limits and of the pull-in and holding range remain the same, because of the network at terminal 15, although the absolute values are modified. If, however, I_{15} is switched, for example by a variation of R_{osc}, the relative values of the three latter magnitudes change as do the absolute values.

A control loop now serves to give the oscillator by means of the current I_R a defined phase position with respect to the shaped sync waveform at terminal 6. For this purpose the oscillator and the sync signal are compared in a phase discriminator, the circuit of which is shown in Fig. 12: it comprises a d.c. comparator, the phase discriminator proper, two controlled current sources, a control-voltage limiter stage and a control-current switching stage. The comparator opens the discriminator if, at its input, terminal 6, there is a voltage which is greater than

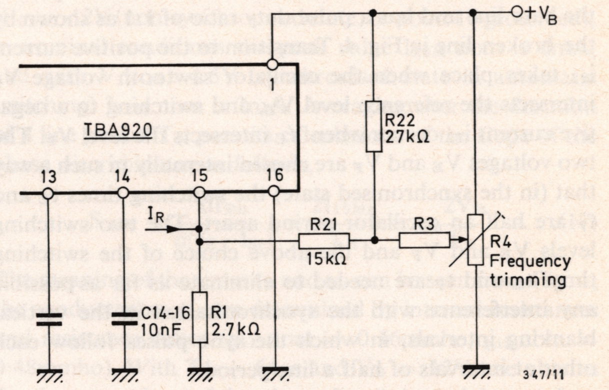

Fig. 11—Network for fine trimming of the free oscillator frequency f_{osc0}

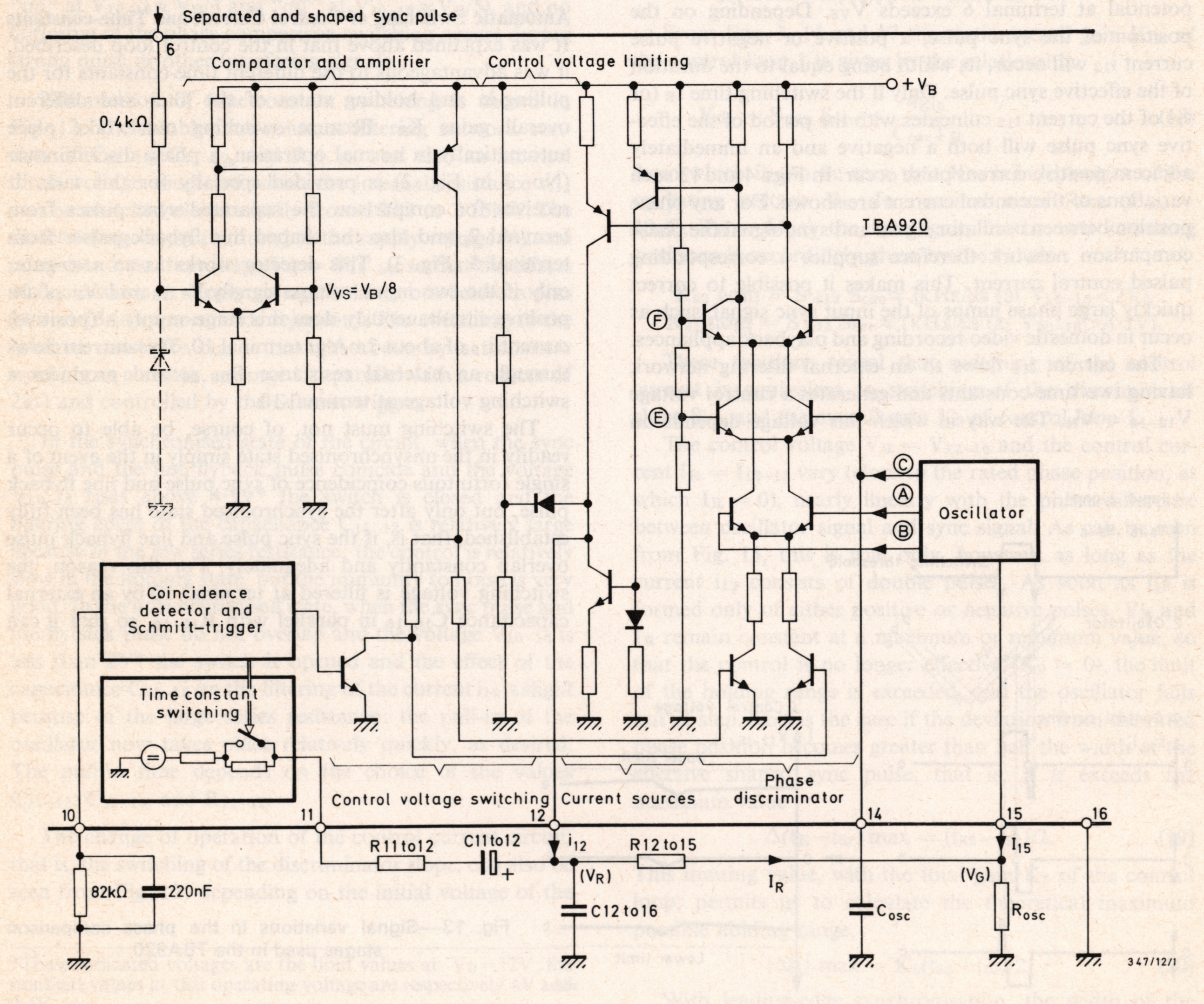

Fig. 12—Circuit for phase comparison of oscillator and sync signal

the reference voltage $V_{VS} = V_B/8$, (where V_{VS} nom = 1·5V). The phase discriminator, which receives in addition the three oscillator signals A, B, and C, drives alternately two current sources which finally supply a control current i_{12} for the frequency control of the oscillator at terminal 12.

If we consider a situation where a direct voltage $V_{6-16} > V_{VS}$ is applied to terminal 6, then i_{12} represents a square-wave current which is symmetrical with respect to the base line and has a pulse duty ratio of 1:1 as shown by the broken line in Fig. 4. Transition to the positive current i_{12} takes place when the oscillator sawtooth voltage V_C intersects the reference level V_E, and switching to a negative current i_{12} occurs when V_C intersects the level V_F. The two voltages V_E and V_F are chosen internally in such a way that (in the synchronised state) the switching times t_E and t_F are half an oscillator period apart. The two switching levels V_E and V_F and the above choice of the switching times t_E and t_F are needed to eliminate as far as possible any interference with the synchronisation in the vertical blanking intervals, in which the sync pulses follow each other at intervals of half a line period.

In normal operation, however, the shaped sync pulse is applied to terminal 6. This pulse restricts the duration of the square-wave current to the time during which the potential at terminal 6 exceeds V_{VS}. Depending on the position of the sync pulse, a positive or negative pulse current i_{12} will occur, its width being equal to the duration of the effective sync pulse. Only if the switching time t_E (or t_F) of the current i_{12} coincides with the period of the effective sync pulse will both a negative and an immediately adjacent positive current pulse occur. In Figs. 4 and 13 such variations of the control current are shown. For any phase position between oscillator signal and sync signal the phase comparison network therefore supplies a corresponding pulsed control current. This makes it possible to correct quickly large phase jumps of the input sync signal, such as occur in domestic video recording and playback appliances.

The current i_{12} flows to an external filtering network having two time-constants and generates a control voltage $V_{12-16} = V_R$. The way in which this voltage depends on the phase position between oscillator signal and sync signal is shown in Fig. 13: the voltage V_{12-15} differs from the voltage V_{12-16} by the constant value V_{15-16} (V_G, Fig. 10). A limiter, provided internally, allows the voltage V_R to fluctuate only between a minimum value of 0·7V and a maximum value of 5·5V. The control voltage V_R generates a control current

$$I_R = \frac{V_{12-15}}{R_{12-15}} = \frac{V_R - V_G}{R_{12-15}}, \qquad \ldots(16)$$

where

$$V_G = V_{15-16}.$$

This is passed to the oscillator for the control of its frequency and phase position via an external resistance $R_{12=15}$ connected across terminals 12 and 15.

Thus the direction of the control current I_R depends upon the phase difference between the oscillation waveform and the shaped sync pulse. A high loop gain and excellent oscillator frequency stability together with small tolerances in the phase characteristics of the phase detector ensure that (assuming the oscillator frequency has been trimmed in advance) the instant t_E (Fig. 4) coincides, to within a few tenths of a microsecond, with the centre of the shaped sync pulse.

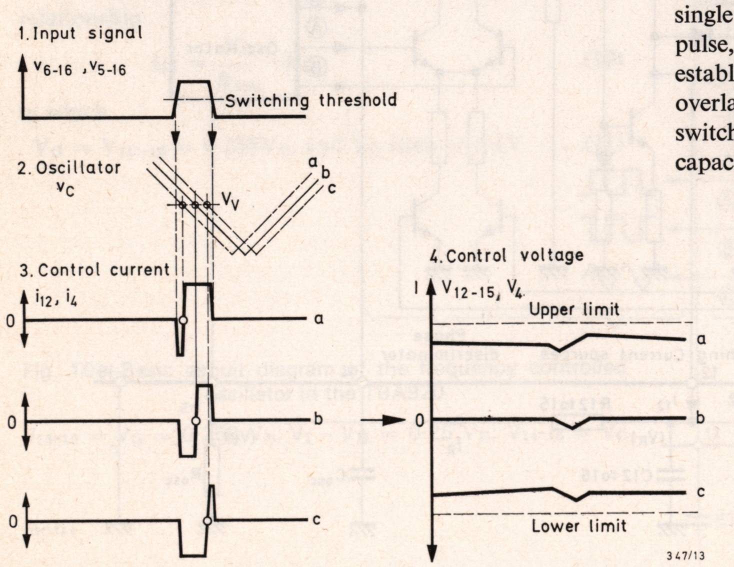

Fig. 13—Signal variations in the phase comparison stages used in the TBA920

Automatic Switching of Control Current and Time-constants

It was explained above that in the control loop described, it was advantageous to use different time-constants for the pulling-in and holding states of the filter and different overall gains K_0. Because switching must take place automatically in normal operation, a phase discriminator (No. 3 in Fig. 2) is provided specially for this task. It receives for comparison the separated sync pulses from terminal 7, and also the shaped line flyback pulses from terminal 5 (Fig. 3). This detector works as an AND-gate; only if the two input voltage signals V_{7-16} and V_{5-16} are positive simultaneously does this stage supply a (positive) current i_{10} of about 2mA at terminal 10. This current flows through an external resistance R_{10-16} and produces a switching voltage at terminal 10.

The switching must not, of course, be able to occur readily in the unsynchronised state simply in the event of a single fortuitous coincidence of sync pulse and line flyback pulse, but only after the synchronised state has been fully established, that is, if the sync pulse and line flyback pulse overlap constantly and adequately. For this reason, the switching voltage is filtered at terminal 10 by an external capacitance C_{10-16} in parallel with R_{10-16}, so that it can change only slowly and the switching, correspondingly delayed, can take place only in the hold state.

If, as a result of a phase jump in the sync signal, or some other interference, the oscillator drops out of step, a certain time elapses, of the order of magnitude of $t_3 = R_{10-16} \times C_{10-16}$, until the voltage V_{10-16} has dropped below the threshold value $V_B/5$ and the circuit is switched over again to optimum pull-in performance. In the operation of domestic video recorders, where line sync phase jumps during the vertical gating interval may occur frequently, this is particularly annoying. With an external switch connected between terminal 10 and earth and closed for V.T.R. operation, the circuit is held in the condition for optimum pull-in performance, regardless of other conditions, so that after a phase jump the oscillator voltage is quickly brought again to the right phase position, as also is the gating pulse for the line output stage.

The switching voltage at terminal 10 does not directly control the phase comparison stage but first drives a Schmitt trigger, and the output of this effects the switching of the time-constant and of the control current in the phase comparison stage; this arrangement ensures that switching takes place at defined threshold values (nominal values: "on" at $V_{10-16} \approx V_B/3$ and "off" at $V_{10-16} \approx V_B/5$), and no fluttering of the phase comparison switching occurs during strong noise or other interfering signals.

The method of time-constant switching is shown in Fig. 12. The double-time-constant filtering network consists of C_{12-16}, C_{11-12}, and R_{11-12}, and also an internal direct voltage source of which the internal resistance r_{i11} can be switched electronically from 150Ω to 2·15kΩ. The direct voltage is proportional to the supply voltage V_B and corresponds to the voltage $V_G = V_{15-16}$, so that the effects of fluctuations in supply voltage balance out between pins 11 and 15 (common-mode rejection). The switching of the internal resistance r_{i11} is brought about by a transistor working as a switch, arranged in parallel with a resistor of 2kΩ and controlled by the Schmitt trigger.

In the synchronised state of the circuit, when the sync pulse and the line flyback pulse coincide and the voltage V_{10-16} rises above 4·5V* the switch is closed and the filtering effect of the capacitance C_{11-12} is relatively large because of the low series resistance; the control is relatively slow in the holding state, but the immunity to noise is very good. In the unsynchronised state, when the sync pulse and the flyback pulse do not overlap and the voltage V_{10-16} is less than 2V* the switch is opened and the effect of the capacitance C_{11-12} on the filtering of the current i_{12} is slight because of the large series resistance: the pull-in of the oscillator now takes place relatively quickly, as desired. The pull-in time depends on the choice of the values C_{11-12}, C_{12-16}, and R_{11-12}.

The change of operation of the control current circuit, that is, the switching of the discriminator slope, can also be seen from Fig. 12: depending on the initial voltage of the Schmitt trigger, the sync pulse causes gating of one or both transistor current sources of the phase discriminator. If both transistors are conducting ($V_{10-16} < 2V$ and $V_{6-16} > 1·5V$), then the current fed into the phase detector and hence also the amplitude of the pulse current i_{12}, is greater than that if only one transistor is switched in ($V_{10-16} > 4·5V$ and $V_{6-16} > 1·5V$). The collector resistances on which the current i_{12} depends, are chosen in the circuit so that, with $V_{10-16} < 2V$ (non-synchronised state, or point 10 grounded), in nominal conditions the peak value I_{12M} nom is 6mA, and with $V_{10-16} > 4·5V$ (synchronised state in automatic switching) I_{12M} nom is 2mA. Averaging over the duration of a line period T_H permits calculations of the slope of the phase discriminator as follows,

$$S_{\phi 1n} = \frac{dI_{Rn}}{d(t_E - t_{Sr})} = \frac{2I_{12Mn}}{T_H} = g_{in}\frac{2V_B}{T_H}. \qquad \ldots(17)$$

The meaning of the times t_E and t_{Sr} can be seen from Fig. 4; the conductances g_{in} are determined by internal resistances and resistance ratios (g_{i1} nom = 0·16mmho, g_{i2} nom = 0·48mmho). With T_H = 64µs and V_B = 12V one obtains for the two values of the phase discriminator slope

$$S_{\phi 12} \text{ nom} \approx 180\mu A/\mu s \text{ at } V_{10-16} < 2V, \text{ and}$$
$$S_{\phi 11} \text{ nom} \approx 60\mu A/\mu s \text{ at } V_{10-16} < 4·5V.$$

From Eqs. 3, 14 and 17 the static overall gain K_{0n} of the control loop 1 is given by the relationship

$$K_{0n} = S_{\phi 1n}\, S_{osc} = \frac{4g_{in}}{C_{osc}T_H}, \qquad \ldots(18)$$

from which it can be seen that K_{0n} is independent of the operating voltage V_B. In nominal conditions (C_{osc} = 10nF, T_H = 64µs) the total gain in the two switching positions is accordingly given by the values

$$K_{02} \text{ nom} = S_{\phi 12}\, S_{osc} \approx 3kHz/\mu s \text{ (at } V_{10-16} < 2V),$$
$$K_{01} \text{ nom} = S_{\phi 11}\, S_{osc} \approx 1kHz/\mu s \text{ (at } V_{10-16} > 4·5V).$$

These relations reveal that switching of the control current is equivalent to switching of the discriminator slope $S_{\phi 1}$ and the overall gain K_0 of control loop 1.

The control voltage $V_R = V_{12-16}$ and the control current $I_R = I_{12-15}$ vary (close to the rated phase position, at which I_R = 0), nearly linearly with the phase difference between oscillator signal and sync signal. As can be seen from Fig. 13, this is true only, however, as long as the current i_{12} consists of double pulses. As soon as i_{12} is formed only of either positive or negative pulses, V_R and I_R remain constant at a maximum or minimum value, so that the control is no longer effective (K_0 = 0), the limit of the holding range is exceeded, and the oscillator falls out of step. This is the case if the deviation from the rated phase position becomes greater than half the width of the effective shaped sync pulse, that is, if it exceeds the maximum value

$$\Delta(t_E - t_{Sr}) \text{ max} = (t_{S2} - t_{S1})/2. \qquad \ldots(19)$$

This limiting value, with the total gain K_0 of the control loop, permits us to calculate the theoretical maximum possible holding range,

$$|\Delta f_1| \text{ max} = K_0(t_{S2} - t_{S1})/2. \qquad \ldots(20)$$

With leading-edge synchronisation, the width of the effective processed sync pulse, based on the circuit values of Fig. 3 or 8, is about 2μs, leading in this case to the following values of the maximum holding range theoretically possible:

---

*These indicated voltages are the limit values at V_B=12V; the nominal values at this operating voltage are respectively 4V and 2.4V.

$$|\Delta f_{11}| \text{ max} = 1\text{kHz at } V_{10-16} > 4{\cdot}5\text{V},$$
$$|\Delta f_{12}| \text{ max} = 3\text{kHz at } V_{10-16} < 2\text{V}.$$

A holding range much in excess of the pull-in range is of no advantage and should in fact be avoided to prevent excessive drawing away of the oscillator frequency on synchronisation to interference originating inside the receiver (such as upper harmonics radiated by the horizontal output stage). The holding range can be reduced by using the control voltage limitation mentioned above. Since the control voltage V_R can lie only in the range of 3·1V±2·4V, it is possible to limit the control current I_R additionally by a sufficiently large resistance R_{12-15}. As soon as this resistance exceeds the value

$$R_{12-15}\text{ min} = \frac{2{\cdot}4\text{V}.\ T_H}{I_{12M}(t_{S2}-t_{S1})}, \qquad \ldots(21)$$

the voltage limitation becomes effective and the holding range is limited to

$$|\Delta f_2| \text{ max} = S_{osc}\, I_R \text{ max} = S_{osc}\frac{2{\cdot}4\text{V}}{R_{12-15}}. \qquad \ldots(22)$$

With the recommended resistance $R_{12-15} = 33\text{k}\Omega$, for example, the nominal holding range is reduced to

$$|\Delta f_2| \text{ max} = 1{\cdot}2\text{kHz},$$

but it becomes effective only at $V_{10-16} < 2\text{V}$ since only in that case is it possible to meet the conditions

$$\left[\begin{array}{l} R_{12-15} > R_{12-15}\text{ min} \\ \text{and} \\ |\Delta f_2| \text{ max} < |\Delta f_1| \text{ max}. \end{array}\right.$$

If the smallest of the three possible holding ranges mentioned above, $|\Delta f_{11}|$ max = 1kHz, is exceeded and provided that $|\Delta f_2|$ max > $|\Delta f_1|$ max($V_{10-16} > 4{\cdot}5$), then in the threshold region (1kHz < $|\Delta f|$ < 1·2kHz) synchronisation failure is not yet total. Because of the automatic switching of the slope $S_{\phi 1}$ of phase discriminator 1 (and hence of the holding range Δf_1 max) only the overall phase position fluctuates by the amount required for the switching of the coincidence detector. Only at $|\Delta f| > |\Delta f_2|$ max does complete synchronisation failure set in.

The pull-in range of the circuit depends on the discriminator slope $S_{\phi 1}$, on the control time-constants (grounded filter connected across terminals 11, 12) and on the limitation of the control current (that is, on $t_{S2}-T_{S1}$) and voltage (if $R_{12-15} > R_{12-15}$ min). The pull-in range should be adapted to the expected frequency tolerances of the oscillator and sync signal, and should cover approximately the holding range. With good interference suppression and short pull-in time this aim can be achieved by an appropriate choice of the four values mentioned above, of which the discriminator slope and the control time-constant can be selected freely because of the provisions made for switching.

Dimensioned examples of the external network at terminals 11, 12, and 15 are shown in Figs. 3 and 9 for leading-edge and mean-pulse synchronisation.

As soon as the supply voltage V_B falls below about 9V, then irrespective of the switching state of the Schmitt trigger (that is, irrespective of the voltage V_{10-16}) the discriminator is switched to a steep slope for phase comparison between the oscillator and the sync signal and the filtering network of control loop 1 is switched to a low filtering effect. This ensures that the oscillator remains synchronised down to a very small operating voltage V_B (depending on the input network at terminal 9 and on the shaping network across terminals 6 and 7). Except for this switching, the main characteristics of the closed control loop 1 are largely independent of the operating voltage.

Pulse shaper, phase discriminator 2, and output stage

The oscillator must supply waveforms for the triggering of the horizontal driving and output stage, and these voltages must have a suitable phase position to allow for the switching delays occurring in the output stage. In the TBA920, therefore, a stage is provided for the pulse shaping of the oscillator voltages, in which the width of the generated pulses can be adjusted by a control voltage. If, for example, the phase position of the trailing edge of the pulse is kept constant in relation to the oscillator waveform, the leading edge of the output pulse will change its phase position when the pulse width varies. Such a pulse shaping stage can therefore also serve simultaneously as an electronically controlled phase corrector.

The circuit of the pulse shaping stage used in the TBA920 is shown in Fig. 14. Essentially it consists of two transistors switching stages in series. One switching stage is driven by the oscillator square-wave (A) and is conducting if the voltage V_A is sufficiently positive (that is, $V_A >$ about 1V). The other switching stage is a comparator stage, in which the oscillator sawtooth (V_C) is compared with the control voltage V_{3-16} connected to terminal 3. This stage acts as a switch which is closed if the oscillator sawtooth voltage is less than the reference voltage V_{3-16}. The voltage at point K and the output voltage at terminal 2 will be positive only if both switching stages are closed, that is, with $V_A > 1\text{V}$ and $V_{3-16} > V_C$. As can be seen from the pulse diagram in Fig. 15, the trailing edge of the output signal is determined by the trailing edge of the oscillator voltage V_A and always coincides with the instant at which the oscillator sawtooth voltage assumes its minimum value $V_C = V_H$. The leading edge of the output pulse occurs when the falling oscillator voltage V_C passes through the level V_{3-16}. The phase position of the leading edge of the output pulse can therefore be shifted as desired to the point required for the line output stage by varying the voltage V_{3-16}.

If the shaping networks for the sync pulses are appropriately dimensioned, the trailing edge of the oscillator voltage V_A, and hence also that of the output voltage V_{2-16}, is 2μs later than the end of the blanking time and therefore 2μs later than the end of the flyback time.

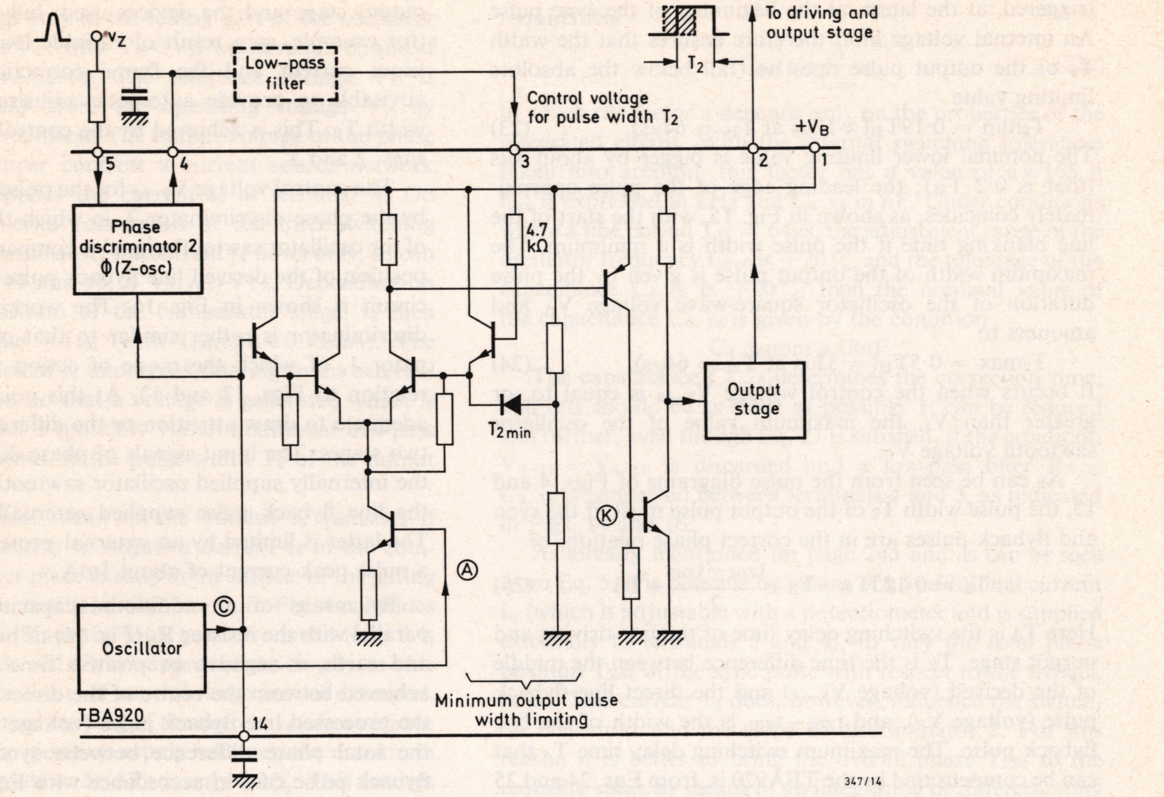

Fig. 14—Network of the pulse shaping stage in which the width T_2 of the pulses generated can be adjusted

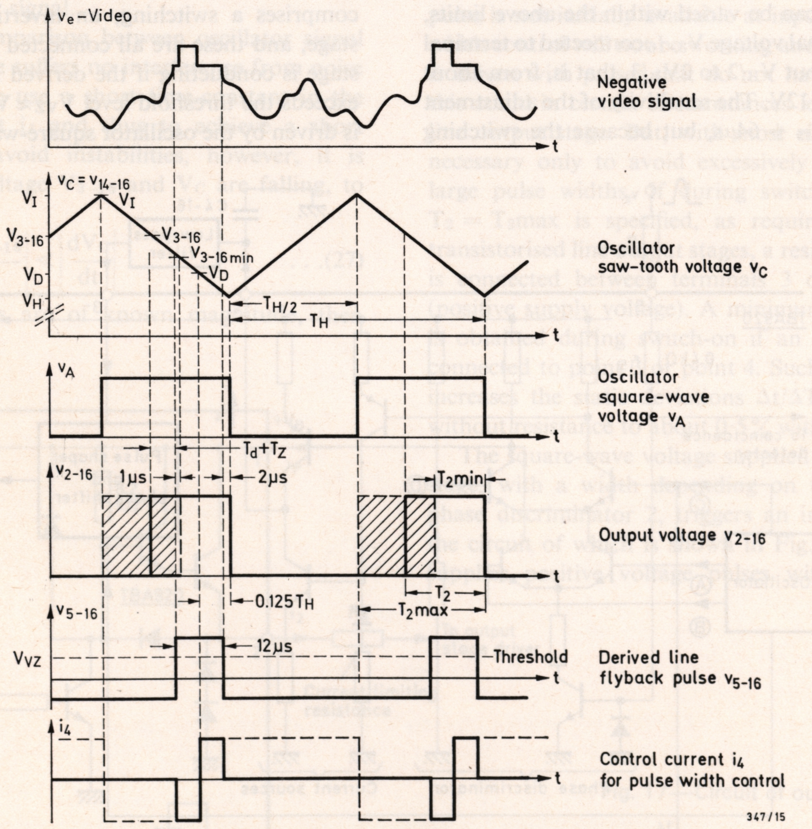

Fig. 15—Pulse/time diagram showing the relative positions of the video signal the oscillator signals V_C and V_A, and the horizontal drive output voltage

The line flyback, on the other hand, must have been triggered, at the latest, at the beginning of the sync pulse An internal voltage limit therefore ensures that the width T_2 of the output pulse does not fall below the absolute limiting value

$$T_{2}\text{min} = 0{\cdot}19T_H (\approx 12\mu s \text{ at } T_H = 64\mu s). \qquad \ldots(23)$$

The nominal lower limiting value is bigger by about 1μs (that is 0·2 T_H); the leading edge of the pulse approximately coincides, as shown in Fig. 15, with the start of the line blanking time if the pulse width is a minimum. The maximum width of the output pulse is given by the pulse duration of the oscillator square-wave voltage V_A and amounts to

$$T_{2}\text{max} = 0{\cdot}5T_H (= 32\mu s \text{ at } T_H = 64\mu s). \qquad \ldots(24)$$

It occurs when the control voltage V_{3-16} is equal to, or greater than V_I, the maximum value of the oscillator sawtooth voltage V_C.

As can be seen from the pulse diagrams of Figs. 4 and 15, the pulse width T_2 of the output pulse must, if the sync and flyback pulses are in the correct phase relation, be

$$T_2 = 0{\cdot}125T_H + T_Z + \frac{t_{Z02} - t_{Z01}}{2} + Td \qquad \ldots(25)$$

Here T_d is the switching delay time of the line driving and output stage, T_Z is the time difference between the middle of the derived (voltage V_{5-16}) and the direct line flyback pulse (voltage V_Z), and $t_{Z02} - t_{Z01}$ is the width of the line flyback pulse. The maximum switching delay time T_d that can be compensated by the TBA920 is, from Eqs. 24 and 25

$$T_{d}\text{max} = 0{\cdot}375T_H - T_Z - \frac{T_{Z02} - t_{Z01}}{2}. \qquad \ldots(26)$$

The pulse width T_2 can be varied within the above limits, by means of an external voltage V_{3-16} connected to terminal 3, in the range of about $V_B/2$ to $2V_B/3$, that is, from about 6V to 8V with $V_B + 12V$. The sensitivity of the adjustment is about 10μ/V at $T_H + 64\mu s$, but because the switching delay times may vary not only according to the type of line output stage and the devices used, but also dynamically (for example, as a result of variable loads caused by the beam current and the frame correction circuit), it is advisable to provide automatic adjustment of the pulse width T_2. This is achieved by the control loop 2 shown in Figs. 2 and 3.

The control voltage V_{3-16} for the pulse width is supplied by the phase discriminator 2, in which the phase position of the oscillator sawtooth signal is compared with the phase position of the derived line flyback pulse at terminal 5; its circuit is shown in Fig. 16. The working of this phase discriminator is rather similar to that of phase discriminator 1, of which the mode of action was explained in relation to Figs. 12 and 13. At this point, it is therefore adequate to draw attention to the differences between the two stages. The input signals of phase discriminator 2 are the internally supplied oscillator sawtooth voltage V_C and the line flyback pulse supplied externally to terminal 5. The latter is limited by an external protection resistor R_s a pulse peak current of about 1mA.

By means of an additional capacitor connected in parallel with the resistor R_s (Fig. 16) or between terminal 5 and earth, a negative or positive time shift T_Z can be achieved between the centre of the direct (voltage V_Z) and the processed line flyback pulse (voltage V_{5-16}). With this the total phase difference between sync pulse and line flyback pulse can, in accordance with Eq. 5, be adjusted. Examples of dimensioned networks appear in Figs. 3 and 9.

As can be seen from Fig. 16, the phase discriminator 2 comprises a switching, an inverting, and a comparator stage, and these are all connected in series. The switching stage is conducting if the derived line flyback pulse V_{5-16} exceeds the threshold level $V_{VZ} \approx V_{BE}$. The inverting stage is driven by the oscillator square-wave voltages V_A and V_B.

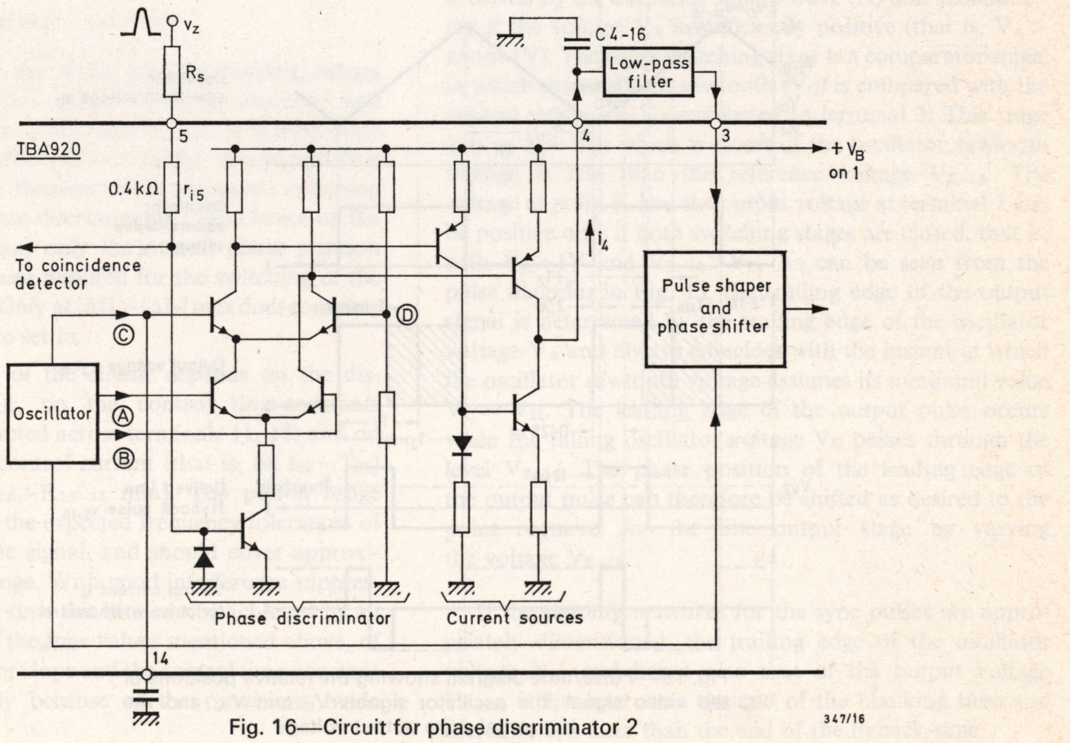

Fig. 16—Circuit for phase discriminator 2

The comparator stage determines the polarity of the output signal i_4, although only in the falling part of the oscillator sawtooth voltage V_C: with $V_C < V_D$ we have $i_4 > 0$, and if $V_C > V_D$ we have $i_4 < 0$. The reference voltage V_D is obtained internally from the operating voltage V_B by means of voltage division. The output voltage of the phase discriminator proper controls a current source network which finally supplies the current i_4 at terminal 4. On account of the series connection of the three switching stages in the discriminator, the current i_4 flows only, as can be seen in Figs. 13 and 15, if $V_{5-16} > V_{VZ}$. Depending on the switching position of the comparator stage, i_4 then assumes the value $\pm I_{4M}$ (with $I_{4M}\text{nom} \approx 0{\cdot}75\text{mA}$). The pulse-shaping current i_4 undergoes filtering in an external capacitance C_{4-16}, so that a voltage is generated which is passed to terminal 3 (possibly via an additional low-pass filter) for the control of the pulse width T_2 of the output voltage V_2.

The arithmetical mean of the current i_4 vanishes if reversal from positive to negative current i_4 in the comparator stage takes place exactly in the middle of the gating line flyback pulse, that is, if the time t_D in Fig. 4 coincides with the time t_{Z5}. Since the loop gain of control loop 2 is large, the network will always approximate closely to this state as long as the limits of control range are not exceeded. If there is no external tapping of the current i_4 (via a resistor to earth or to the positive supply voltage), the maximum relative static deviation $\Delta t/\Delta T_d$ is only 0·2%. This ensures that the middle of the (shaped) line flyback pulse, has within close tolerances, a certain given phase position with respect to the oscillator signal.

Since the phase comparison between oscillator signal and line flyback voltage suffers no interference from noise signals it is possible to use a short time-constant in the filtering of the current i_4 and thus to achieve a short correction time. To avoid instabilities, however, it is necessary when the voltage V_{3-16} and V_C are falling, to ensure that

$$\left|\frac{dV_{3-16}}{dt}\right| < \left|\frac{dV_C}{dt}\right| \qquad \ldots(27)$$

If these differentials are of known magnitude, then under the condition $V_{4-16} = V_{3-16}$ there arises the requirement

$$C_{4-16} > \frac{a}{f_{osc}} \qquad \ldots(27a)$$

in which the factor a depends only on the properties of the integrated circuit. With the internal switching tolerances taken into account, this factor has a value of $a \approx 165$ if f_{osc} is expressed in kHz and C_{4-16} in nF. Under conditions where a line period $T_H = 64\mu s$, the adjustment range of the oscillator frequency f_{osc0} is ±20%, and the tolerance of the capacitance C_{4-16} is ±20%, then the nominal value of the capacitance C_{4-16} is given by the condition

$$C_{4-16}\text{nom} \geqslant 18\text{nF}.$$

The capacitance C_{4-16} determines the correction time, and this should be as short as possible. It can be reduced still further, even though Eq. 27 is satisfied, if the condition $V_{4-16} = V_{3-16}$ is discarded and a low-pass filter R_{3-4}, C_{3-16} is connected between terminals 4 and 3, as indicated in Figs. 14 and 16.

As already mentioned on page 245 and as can be seen from Eq. 5, it is possible by means of an additional current I_q (which is adjustable with a potentiometer and is supplied externally to terminals 3 and 4), to vary the total phase position T_{ZSr} of the sync pulse with respect to the flyback pulse. This current I_q does, however, influence the switch-on behaviour and the slope of discriminator 2. For this reason it is better to bring the overall phase T_{ZSr} to the requisite value by means of an integrating or differentiating network connected to terminal 5.

When the receiver is first switched on, the line flyback pulse is not initially available at input 5, and so the pulse width control will not be working and the line output stage is driven with pulses that do not have the correct width; this could in certain circumstances lead to damage of the line output stage. But, with most circuits, it is generally necessary only to avoid excessively small or excessively large pulse widths. If during switch-on, a pulse width $T_2 = T_{2}\text{max}$ is specified, as required, for example, in transistorised line output stages, a resistance $R_{3-1} < 2{\cdot}2M\Omega$ is connected between terminals 3 or 4 and terminal 1 (positive supply voltage). A minimum pulse width $T_{2}\text{min}$ is obtained during switch-on if an earthed resistance is connected to point 3 or point 4. Such a resistor, however, increases the static deviations $\Delta t/\Delta T_d$ from about 0·2% without resistance to about 0·5% with $R = 2{\cdot}2M\Omega$.

The square-wave voltage supplied by the pulse shaping stage, with a width depending on the output signal of phase discriminator 2, triggers an internal output stage, the circuit of which is shown in Fig. 17. At terminal 2 it supplies positive voltage pulses with $V_{2M} = 10V$ at a

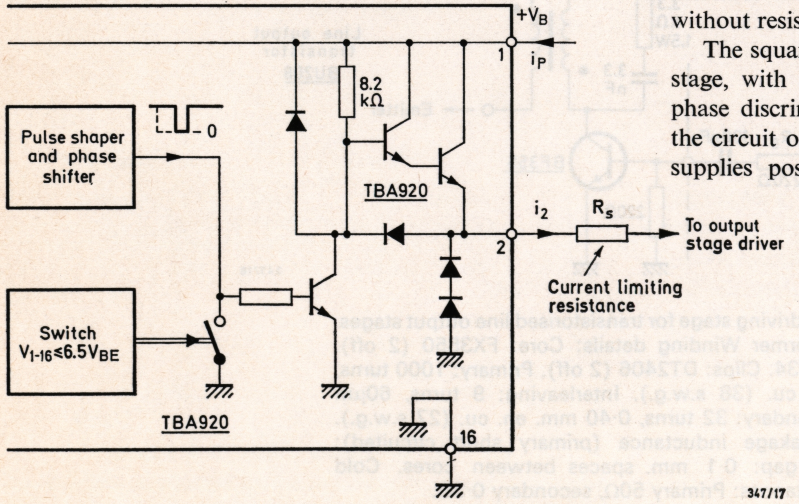

Fig. 17—Circuit of output stage of TBA920

maximum mean output current $I_2max = 20mA$ ($I_{2M} = 200mA$) for the triggering of the line driver stage. A push-pull output stage is used with additional protective diodes connected between output 2 and earth and the terminal for the positive supply voltage. In either switching state the output stage has at the output a low internal resistance of a few ohms. Limitation of the output current is achieved by an external resistance between terminal 2 and the network connected to it. In case of direct short-circuiting between terminals 2 and 1 or 16 there is a risk of damage. For particularly rapid switching this resistance can be partially bridged capacitively, but it is essential to observe the limiting values of the output current i_2.

The design of the ouput stage network (push-pull with protective diodes and external limiting resistance) ensures the best possible degree of protection against e.h.t. flash-over discharges and accidental short-circuits.

At supply voltages of less than $V_B \approx 6{\cdot}5V_{BE} (= 4{\cdot}3V$ at $0 = 25°C$) the output stage is blocked in the "on", switching state, so that further driving of the line output stage ceases. At least up to this limiting value of V_B the oscillator works in the linear modulation range with a definite frequency deviation of $|\Delta f_{osc0}/f_{osc0}| < 10\%$ in terms of the value at $V_B = 12V$. For spot suppression on switching off, the wide range of operating voltage from $V_B = 12V$(nom) (13·2Vmax) to $V_B \approx 6{\cdot}5V_{BE}$ is therefore available.

Supply voltage

The operating voltage $V_B = V_{1-16}$ for the TBA920 can, for normal operation, lie in the range 10V to 13·2V. The current consumption of the integrated circuit with nominal supply voltage at terminal 1 consists of the internal current and the output current i_2, and the nominal value is given by $i_p = i_2 + 36mA$ (Fig. 17). The spread on the value of internal current is ±25%, that is ±9mA.

If the supply voltage for the TBA920 is obtained via a scan rectifier network from the line output stage, then for the period immediately following switch-on, a supply from the mains unit (or another voltage source) must be provided. As soon as the requisite direct voltage is supplied via the line output stage, automatic switching of the operating voltage can take place by means of a transfer diode.

If a power supply for starting the TBA920 is obtained with a series dropping resistor from the main h.t. line in the receiver, the starting requirement for the TBA920 internal circuit is $18mA \pm 4{\cdot}5mA = 22{\cdot}5mA$ max. A further allowance must be made for the current taken by the coupling network to the line driver transistor; to estimate this a supply voltage during starting of about 6V can be assumed. If, in a particular case, the mean drive network current is 2·5mA at $V_B = 6V$ then the design must be for a total required starting current of $22{\cdot}5 + 2{\cdot}5 = 25mA$. The dropping resistor will continue to supply substantially this current after switch-on, therefore a continuous power rating based upon the 25mA requirement is necessary. After switch-on the remaining current required, corresponding to $V_B = 12V$, is supplied from the transfer diode.

Terminal 13, the decoupling point for the oscillator voltage reference network can be decoupled to earth in cases where the presence of ripple on the l.t. supply causes appreciable horizontal phase modulation. In such cases, to prevent momentary overdriving of the oscillator circuit during switch-on and switch-off, the time-constant of the l.t. supply voltage source should be about ten times the time-constant C_{13-16}, R_{i13} with $R_{i13} = 1{\cdot}8k\Omega$. Decoupling of the integrated circuit from the main l.t. supply can be achieved appropriately by the incorporation of a CR filter, of about $R_V = 10\Omega$ and $C_{1-16} = 100\mu F$, in the (positive) operating voltage line, as shown in Fig. 3. If such a filter is used, a supply voltage of $V_B = 12V \pm 10\%$ is recommended.

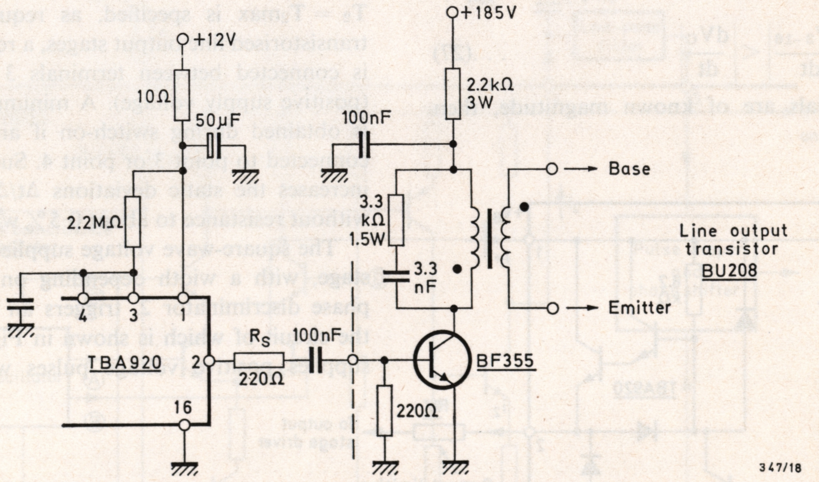

Fig. 18—H.T. driving stage for transistorised line output stages. Driver Transformer Winding details: Core: FX3550 (2 off). Bobbin: DT2534. Clips: DT2406 (2 off). Primary: 1000 turns, 0·14mm. en. cu. (38 s.w.g.). Interleaving: 9 turns, 60μm Melinex. Secondary: 32 turns, 0·40 mm. en. cu. (27 s.w.g.). Secondary leakage inductance (primary short circuited): 16·6μH. Air gap: 0·1 mm. spaces between cores. Cold resistances: Primary 50Ω, secondary 0·3Ω.

However, in cases where the l.t. supply is already well filtered C_{13-16} can be dispensed with.

An example of a driving stage for the line output transistor, operating from the main h.t. supply in the receiver, is shown in Fig. 18.

Board layout and adjustment

The external wiring of the TBA920 is reasonably non-critical but the following recommendations should be noted:

a) C_{1-16} should be connected by short low-resistance leads between terminals 1 and 16 to achieve the best possible decoupling.
b) C_{13-16}, C_{14-16}, and R_{15-16}: a common low-resistance earthing line should be used at terminal 16, separated, if possible, from the other earthing lines, to prevent coupling of interference signals.
c) The decoupling resistances of the outputs 2 and 7 should be connected directly to the terminals of the integrated circuit. This minimises the possibility of damage due to short-circuiting.
d) The input video signal should be supplied via a screened lead, grounded at both ends for minimum coupling of interference signals capacitively, inductively, or by earth coupling, and for protection in case of e.h.t. flashovers.
e) The types of current limitation resistances at terminals 1, 5, and 7 should be chosen so that current limitation is effective also in case of e.h.t. flashovers.

The adjustment of the requisite time difference T_{ZSr} between the middle of the line flyback pulse and the leading edge of the sync pulse, as given by Eq. 9 can be achieved by a time shift T_Z of the line flyback pulse with the help of a differentiating or integrating network before input 5 or an additional current I_q fed externally to terminal 3 and 4 in accordance with Eq. 5. Attention must be paid to the fact that T_Z or I_q depends on T_{ZSr} as well as on the delay times T_{S1} and T_{S2} brought about by the processing network for the coupling and sync pulse. If the tolerances of the external network are kept sufficiently small, an individual adjustment of the time I_{ZSr} is normally unnecessary.

On the other hand it will generally not be possible to avoid individual trimming of the free oscillator frequency f_{osc0}. This is done most appropriately by adjustment of the closed-circuit current $I_{15,0}$ (at control current $I_R = 0$) by means of an external trimming resistance (Figs. 3 and 11). To ensure that during such trimming there is no flow of the control current I_R, terminal 6 should be temporarily connected to earth.

Thus trimming of the horizontal combination TBA920 presents no difficulties and can be performed quickly and easily.

Simple low-power temperature stabilizer

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A simple temperature stabilizer for controlling the temperature of any small electronic component mounted in a metal block is described. The circuit maintains the block temperature constant to within ±0·5degC for a change in ambient temperature of 0 to 40°C, or a change in supply voltage of 8 to 16V.

INTRODUCTION

The low-power temperature stabilizer described in this article can be used to control the temperature of any small electronic component, for example a quartz crystal. The circuit utilizes an NTC 'two-point' thermistor as the temperature sensor and operates from any supply voltage between 8 and 16V.

CIRCUIT DESCRIPTION

The circuit of the temperature stabilizer is shown in Fig. 1. Three resistors R_1, R_2, and R_3, and a 'two-point' NTC thermistor R_4 are connected to form a bridge across the supply. The thermistor is clamped to a small copper or aluminium block which acts as the mounting block for the device whose temperature is to be controlled. The out-of-balance bridge voltage, which is dependent on the temperature of the thermistor and hence that of the block, is applied to the signal input terminals of a TBA221 operational amplifier.

The amplifier operates open-loop and acts as a voltage comparator with very low hysteresis. It switches the collector current of the BD132 transistor on or off, depending on whether the block temperature is below or above the desired value. For simplicity, and because the power required is low, the transistor itself is used as the heater and is attached to the block as close to the thermistor as possible. This is necessary to reduce the thermal resistance between the transistor and the thermistor to a small value and thus minimize 'hunting' of the block temperature about the correct value.

Resistors R_1 and R_2 are made equal because the mean voltage at the input terminals of the TBA221 is required to be one half of the supply voltage. Similarly, R_3 is made equal to the resistance of the thermistor R_4 at the required block temperature. Further, to minimize the effects of the input offset current of the TBA221, the resistances of both arms of the bridge are also made equal. Thus the values of R_1, R_2, and R_3 are made equal to R_4, the nominal thermistor resistance at the required temperature.

The output voltage of the TBA221 switches between about 0·5V and a higher level within 0·5V of the supply voltage. The 4·7kΩ resistor R_5 limits the base current of the BD132 transistor to about 3mA at a supply voltage of 15V. Under these conditions, the current gain of the BD132 is between 40 and 235 and the collector current is between 120 and 705mA.

A single screw is sufficient to bolt the TO-126 envelope of the BD132 transistor to the block. The resultant thermal resistance between collector and block $R_{th(j-b)}$ is 7deg C/W. The maximum junction temperature of the transistor T_j max is 150°C, and the maximum dissipation for mounting base temperatures less than 60°C is 15W. For any block temperature T_b the maximum permissible dissipation is given by:

$$P_{max} = \frac{T_{j}\,max - T_b}{R_{th\,(j-b)}}.$$

For example, if the required block temperature is 90°C, P_{max} is 9W.

If electrical isolation between the collector and the block is necessary, it can be provided by a thin mica washer placed between the transistor and the block. However, this increases the thermal resistance between the block and the mounting base of the transistor and results in a reduced maximum block temperature for a given mean dissipation.

An n-p-n transistor, such as the BD131 (also in a TO-126 encapsulation), can be used in place of the BD132. In this case, however, the transistor collector, which is connected to the positive supply, must be electrically insulated from the block, if the block is earthed. Also, the inputs to the TBA221 need to be reversed with respect to the bridge outputs, to maintain the feedback in the correct sense.

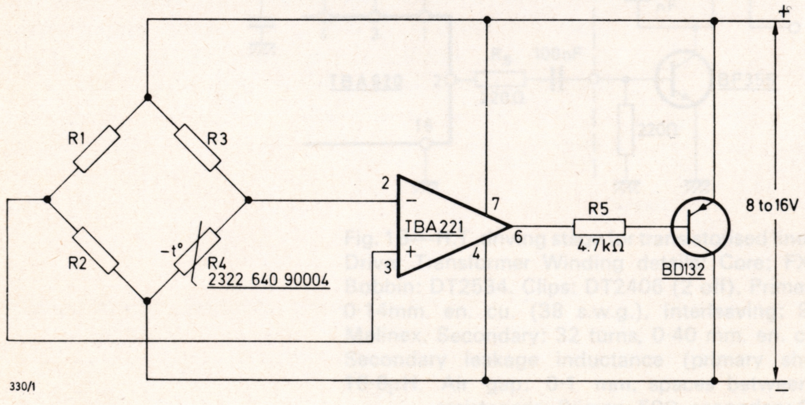

Fig. 1—Simple temperature stabilizer

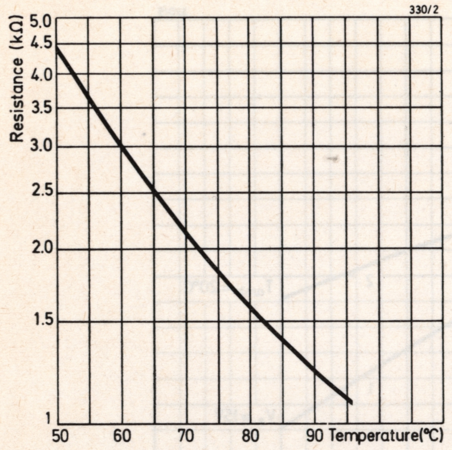

Fig. 2—Resistance of the 2322 640 90004 thermistor plotted against temperature

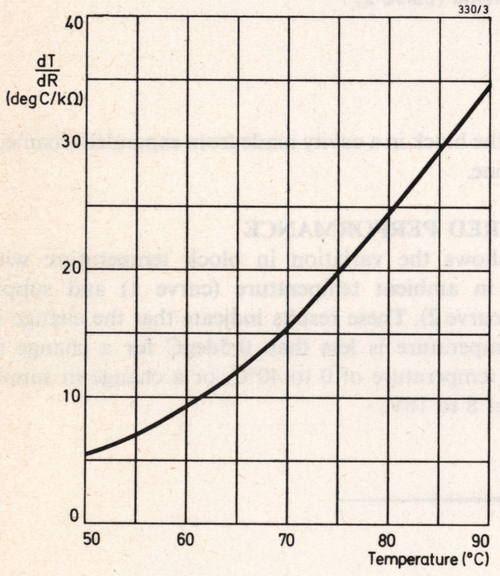

Fig.3—dT/dR plotted against temperature for the thermistor, type 2322 640 90004

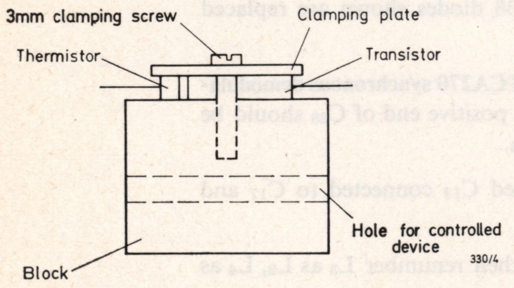

Fig. 4—One arrangement of transistor, thermistor, and block

EFFECTS OF THERMISTOR AND RESISTOR TOLERANCES

It was stated earlier than R_1, R_2, and R_3 are made equal to R_4, the nominal resistance of the thermistor at the required temperature. Fig. 2 shows part of the published resistance temperature characteristic for the 2322 640 90004 thermistor. The nominal thermistor resistance R_{nom} at the required temperature is read from this curve. The spread in the thermistor resistance is ±7%. Therefore, the maximum tolerance on R_{nom} is:

$$\Delta R = R_{nom} \times 0{\cdot}07.$$

Fig. 3 shows dT/dR plotted against temperature. At the required temperature,

$$\Delta T = \Delta R\frac{dT}{dR}.$$

To allow for the spreads of the other resistors (R_1, R_2, and R_3), twice the tolerance of one of these resistors is added to the thermistor tolerance to give an overall tolerance ΔR′. The maximum temperature spread is then:

$$\Delta T_{max} = \Delta R'\frac{dT}{dR}.$$

For example, if the tolerance on the resistors R_1, R_2, and R_3 is 1%,

$$\Delta R' = 7\% + (2 \times 1\%) = 9\%.$$

If the controlled temperature is required to be 70°C, Fig. 2 shows that R_{nom} is 2·2kΩ. With 1% resistors,

$$\begin{aligned}\Delta R &= 2{\cdot}2[0{\cdot}07 + (2 \times 0{\cdot}01)],\\ &= 0{\cdot}198\text{k}\Omega.\end{aligned}$$

But, from Fig. 2, dT/dR at 70°C is 15·5degC/kΩ. Therefore,

$$\begin{aligned}\Delta T_{max} &= 0{\cdot}198 \times 15{\cdot}5.\\ &= 3{\cdot}1\text{degC}.\end{aligned}$$

Similarly, it can be shown that at 50°C, ΔT_{max} = 2·2degC and at 90°C, ΔT_{max} = 3·8degC. If the block is required to operate exactly at the nominal temperature, a pre-set potentiometer can be inserted in the bridge to allow adjustment of R_3.

ASSEMBLY

Fig. 4 shows one arrangement of block, transistor, and thermistor for stabilizing the temperature of a small device. The device is housed in a hole drilled through the block, and the space between the device envelope and the block is

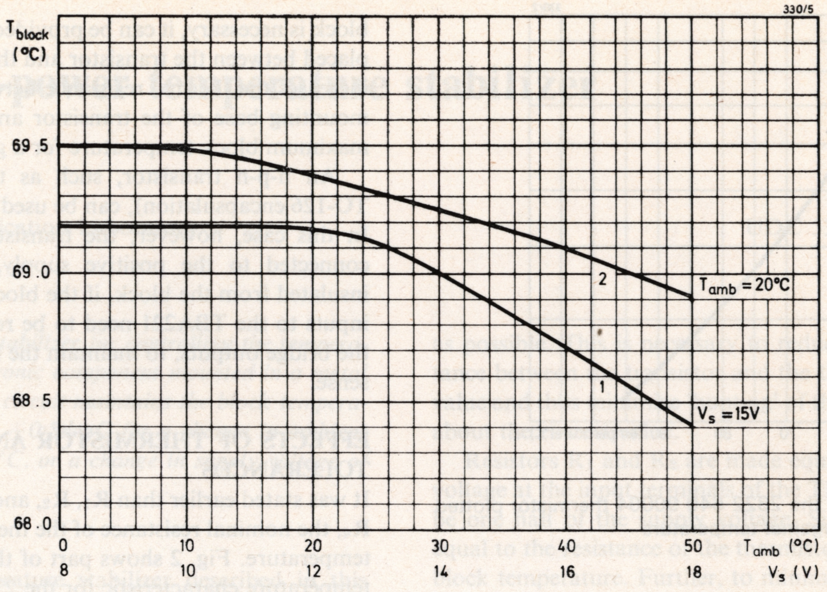

Fig. 5—Variation of block temperature with ambient temperature (curve 1), and supply voltage (curve 2)

filled with heatsink compound. The transistor and the thermistor are clamped to the block by a plate and a single 3mm screw driven into a tapped hole. This method is possible because the thicknesses of the transistor and the thermistor are identical to within 0·1mm.

To reduce the time required for the block to heat up, and also to minimize the power required to maintain the working temperature, it is necessary to make the heat loss from the block to its surroundings as small as possible. This can be achieved in a number of ways, one of which is to place the block in a cavity made from expanded (foamed) polystyrene.

MEASURED PERFORMANCE

Fig. 5 shows the variation in block temperature with changes in ambient temperature (curve 1) and supply voltage (curve 2). These results indicate that the change in block temperature is less than 0·5degC for a change in ambient temperature of 0 to 40°C, or a change in supply voltage of 8 to 16V.

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'Operation and performance of a single-phase and a three-phase bridge inverter' pp 206 to 222. The BAX78 diodes shown in this circuit are now replaced by BAV10 diodes, and the BAY38 diodes shown are replaced by BAW62.

'Television front-end using integrated circuit TCA270 synchronous demodulator' pp 223 to 231. *Page 228, Fig. 11*—The positive end of C_{28} should be connected to the junction of R_2, R_3 and R_4.

Page 230, Fig. 13—The capacitor numbered C_{13} connected to C_{17} and L_5 should be numbered C_{16}.

Page 231, components list—Delete L_2 and then renumber L_3 as L_2, L_4 as L_3, L_5 as L_4, L_6 as L_5, and L_7 as L_6.
C_{100} and C_{124} should both be 2·5pF feedthrough capacitors.